Service Manual

MP MASTER
MA29275

Level Generator

PS-60

Frequency range 6 kHz to 18.6 MHz

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Frequency range 6 kHz to 18.6 MHz

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6. PRELIMINARY REMARKS TO SERVICE MANUAL

Paragraphs 6.1. to 6.4. explain the abbreviations, symbols and schemes in the service manual and in the appendix. Para. 6.5. contains information as to measurement agents, para. 6.6. explains ordering of repair components.

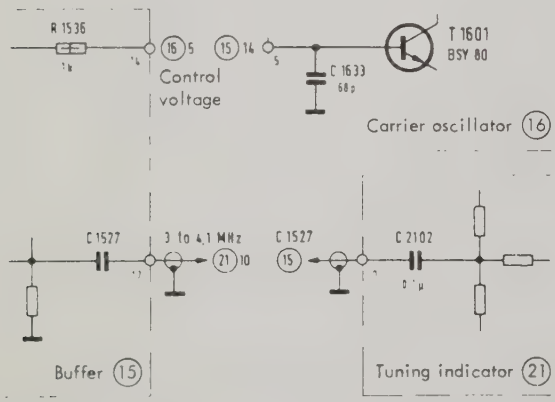
6.1. Circuit elements-key

The modular groups or circuit diagrams are identified with consecutive numbers, e.g. counter (21) . The position numbers of all the circuit elements located within this module unit are indicated with the number 21. The next two figures provide consecutive numbers, for the circuit components, e.g. 06 for a capacitor C 2106 or 11 for resistor R 2111. The leading letters designate the type of circuit component.

IC	21	20	/4.1 — Consecutive number of the IC network
Integr. circuit	Circuit diagram (21)	Consecutive number 20	Count of networks involved with IC (only used with IC's)

6.2. Interconnection between Sub-assemblies

Since the circuit diagrams are given separately for each sub-assembly, it is important that all interconnections are shown clearly. The following drawing explains the method used in this manual.



The drawing shows a connection from point 14 of sub-assembly (15) to point 5 of sub-assembly (16) as well as a screened connection from point 17 of sub-assembly (15) to point 10 of sub-assembly (21) .

6.3. Color code

Color code for resistors and capacitors.

Color	First and Second ring	Third ring	Fourth ring	Fifth [1] ring
	First a and Second number	number of zeros	Tolerance in %	Voltage rating
Black	0	0		
Brown	1	1	1	100
Red	2	2	2	200
Orange	3	3	3	300
Yellow	4	4	4	400
Green	5	5	5	500
Blue	6	6	6	600
Violet	7	7	7	700
Grey	8	8	8	800
White	9	9	9	900
Gold		x0.1 [2]	5	1000
Silver		x0.01 [2]	10	2000
Colorless			20	500

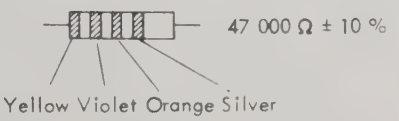
1) Only used for capacitors

2) Multiplier for values under 10

Capacitors are usually marked with a row of colored dots or else rings as with resistors. The row starts at the dot closest to one end of the capacitor.

Resistors are marked usually with rings starting at the head. Usually the body of the resistor is used as the first color point, and as second point a cap. The third point (number of zeros) is a point or ring on the body of the resistor (not used when the ring and the body are the same color.) The tolerance is identified by the color of the second cap.

Example :



6. PRELIMINARY REMARKS TO SERVICE MANUAL

Abbreviations used for hook-up wire colours

bl	blue	rs	pink
bk	uninsulated	rt	red
br	brown	Schirm	shield
fl	transparent	sw	black
ge	yellow	vio	violet
gn	green	ws	white
gr	grey	wsbl	white/blue

6.4. Abbreviations and Symbols

To provide a clearer view in text and circuit diagrams, the following abbreviations and symbols are used:

6.4.1. Discrete components

Battery	B	
Connector/Plug	Bu/St	
Diode, rectifier	Gl	
Zener diode	Gl	
Thyristot	Gl	
Voltage controlled capacitor (Varicap)		
Inductance	L	
Meter	J	
Capacitor	C	
Electrolytic capacitor	C	
Resistor	R	
Negative temperature coefficient resistor	R	
Potentiometer	P	
Crystal	Q	
Relay	Rel	
Relay contact	rel	
Switch	S	
Fuse	Si	
Indicator lamp	SL	

Transistor	T	
Bipolar transistor (Unijunction, FET)	T	
Transformer	Ü	

6.4.2. Digital symbols

See booklet "Digital Primer", chapter 6, Digital Circuits and Symbols.

6.5. Measuring materials

Measuring materials for localizing defects and for verifying voltages, signals, pulses etc. are suggested in the following list:

Level Measuring Setup PSM-5	BN 444/0 W&G
Level Measuring Setup PSM-7	W&G
Milliwatt Test Set EPM-1	BN 564/0 W&G
with Test Probe TK-10	BN 572/0 W&G
Attenuation Network 75 Ω	BN 594/1 W&G
RF Millivoltmeter 411 A	HP
Return Loss Coefficient Bridge R 273	Siemens

6.6. Ordering spare parts

The most important locations for information pertaining to needed spare parts are the spare parts lists. Circuit component numbers prefixed with Bv or WN are to be requested from the manufacturer. The order number (BN) prefixes the equipment number which is located on the lower part of the left handle of the set; additionally for complete plug-in cards, the type and identifying letter; for complete sub-assemblies, the position number. Complete ordering information is seen as follows:

BN 610 No. 430 364 A/T 102

7. FAULT LOCALIZATION AND REPAIR INSTRUCTIONS

Caution: Before opening the Set, disconnect a.c. line plug.

Chapter 5. "Maintenance and General Information" of the "Description and Operating Manual" must be studied and understood as a prerequisite before opening set.

7.1. Disassembly of the PS-60

7.1.1. Removing equipment panels

The equipment panels are fastened with 4 pressure clamps on the back panel. Each panel may be taken off after the two corresponding pressure clamps have been removed. In order to remove the back panel, 2 screws in addition to to the clamps must be unscrewed.

7.1.2. Removing control knobs

After the knob cover cap has been taken off, the screw in the centre of the knob should be removed (special tool order no. W 9, W 20 or W 21). Thereupon the knob may be pulled off the shaft. However, if the clamping cone does not release by itself, then a light tap against the loosened screw should release the knob.

7.1.3. Disassembling the front panel

After the upper and lower equipment panels have been removed, the countersunk screws of the upper and lower trimming strips are unscrewed and removed. As a consequence, the case frame members are exposed, and machine screws are accessible and can be unscrewed at the upper and lower sides. Now the front panel unit can be pulled forward, but care must be taken to protect the cable connections against being damaged.

7.1.4. Opening and disassembly of fold-out chassis

In order to offer easy access to the subassemblies located at the center of the PS-60, the 50 kHz section (7) is constructed as a fold-out chassis. If the two fastening screws are removed from the sides and the drive coupling disconnected from the indicator range switch, then the chassis may be swung out upwards.

For measuring or changing components, the fold-out chassis can be completely taken off the main chassis. For this purpose, the chassis should folded backwards, both the "Subminax" plug on the bottom of the chassis as well as the Amphenol multiple connector should be disconnected, and additionally the rear hinge screws should be unscrewed. See fig. 7-1.

7.1.5. Disassembling printed circuits

First remove cover from the corresponding compartment, then unsolder the connecting wires and unscrew the fastening screws at the printed circuit board.

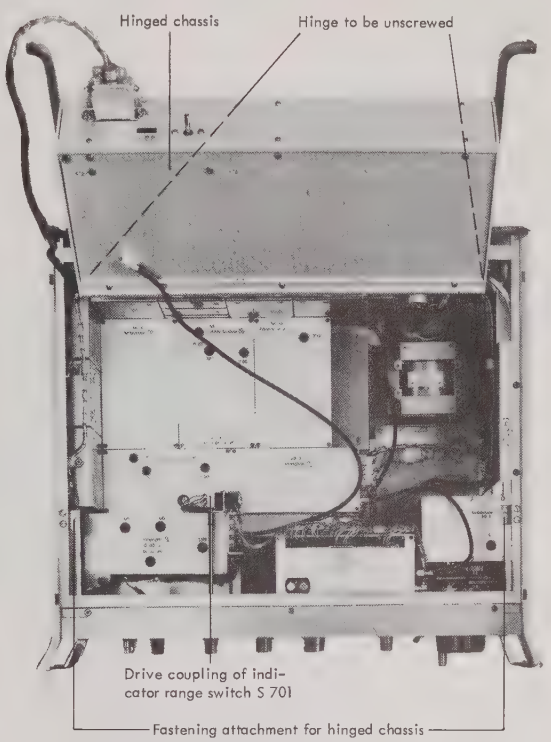

Hinged chassis
Hinge to be unscrewed
Drive coupling of indicator range switch S 701
Fastening attachment for hinged chassis

Fig. 7-1

7.2. Servicing equipment sections

General information for service and maintenance is located in Chapter 5 of the "Operating Manual".

7.2.1. Mechanical drive for frequency settings

If the drive assembly requires service, then it should be oiled, sparingly. Use precision Oil No.28/2,5 E supplied by the firm Riedel, Freiburg, Germany.

7.2.2. Cleaning the output level switch

For this purpose, after first marking the connecting wires and then unsoldering them, the fastening screws are unscrewed to permit removing the switch. The switch should be rotated to "full stop" position, additionally the positions of the contact pins should be noticed. An Allen wrench is used to loosen the screws of the contact pin holder. The holder then can be easily pulled away. Cleaning the contact surfaces is done advantageously with a clean, soft cloth or else a soft rubber eraser could be used. (DO NOT USE CLEANING FLUID).

7. FAULT LOCALIZATION AND REPAIR INSTRUCTIONS

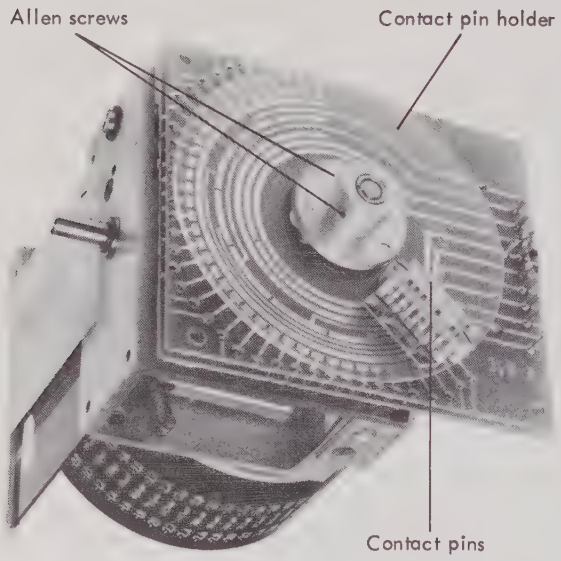


Fig. 7-2

7.3. Safety precautions

7.3.1. Power supply

The PS-60 conforms with protective class I (according to IEC Publ. 348) because the protective ground lead is connected to the instrument chassis or the case.

7.4. Locations of sub-assemblies and test points

Figs. 7-3 to 7-6 illustrate the locations of sub-assemblies and test points.

7.5. Plan for systematic localizing of defects

The following section contains information enabling systematic fault tracing as well as localizing defects within a definite sub-assembly.

With that, a level plan is used instead of the block diagram, and nominal values along the signal path are checked at various test points. The signals generated internally within the instrument may be measured also at test points so that an oscilloscope provides signal forms which from sub-assembly to sub-assembly can be compared to tabulated magnitudes and nominal wave shapes illustrated in the following pages.

The additional relay plan offers conclusive information about the switched status of each relay correlated with the various operating states of the PS-60.

If the defect can be localized at a definite sub-assembly, then from that information the defect is sought within the sub-assembly, moreover help is furnished by the relevant circuit diagram plus the description of the pertinant sub-assembly.

However, it is very important to take into account that all values given on the previously mentioned plans are solely to trace functional defects and are not given as aids for locating tolerance errors.

A tolerance error is defined as a violation of guaranteed accuracy limits without thereby causing any disturbance to rated values for the functions of the Set, e.g: level error is larger by + 0.05 dB than the guaranteed value.

See following level and relay plans as well as table of oscilloscope traces.

adjusted atten-uation dB	Rel 601	Rel 602	Rel 603	Rel 604	Rel 605	Rel 606
0	x		x			
10	x			x		
20	x				x	
30	x					x
40		x	x			
50		x		x		
60		x			x	
70		x				x

PS-60/BN 610
Relay plan

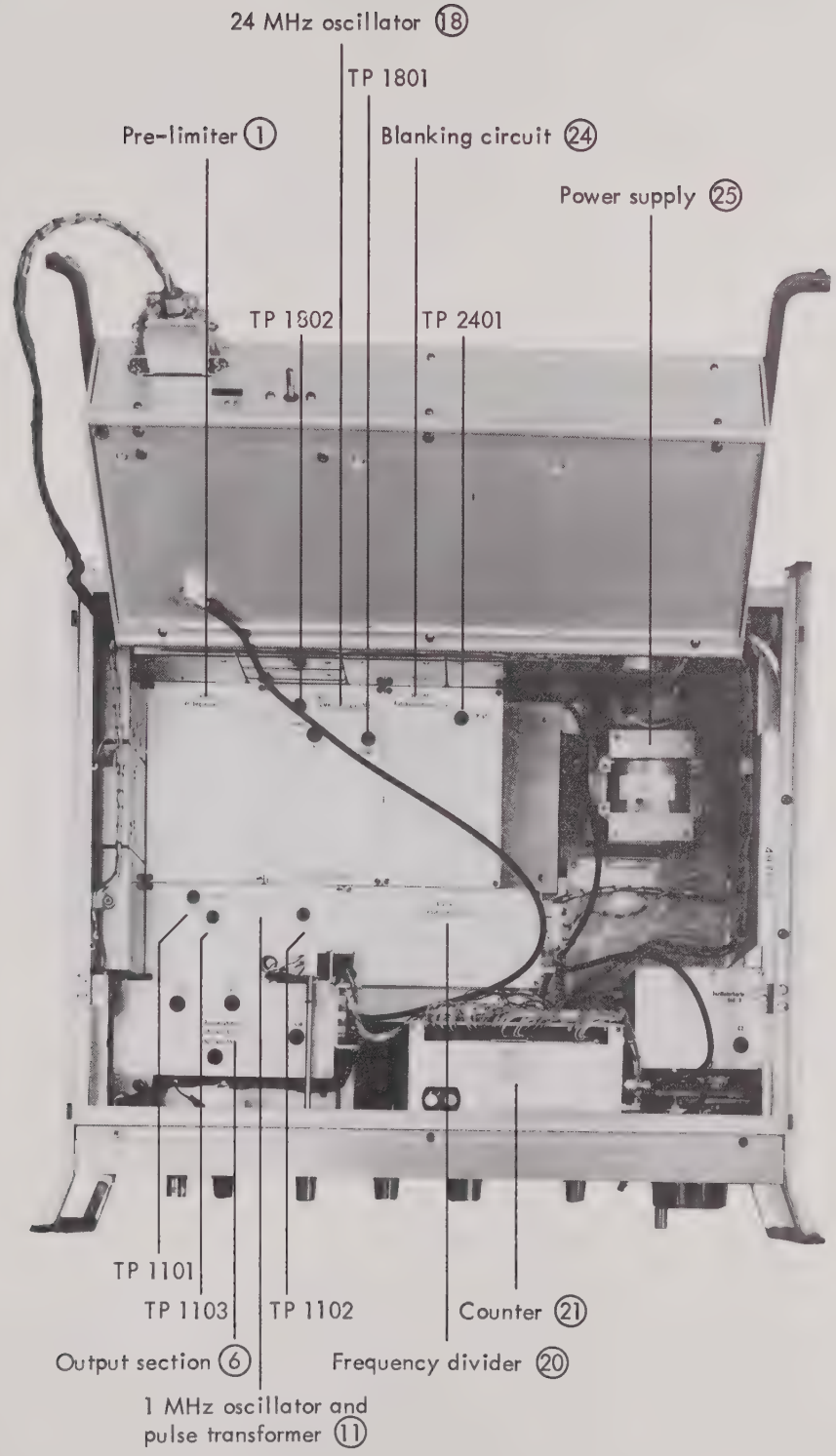


Fig. 7-3 Top view with hinged chassis open

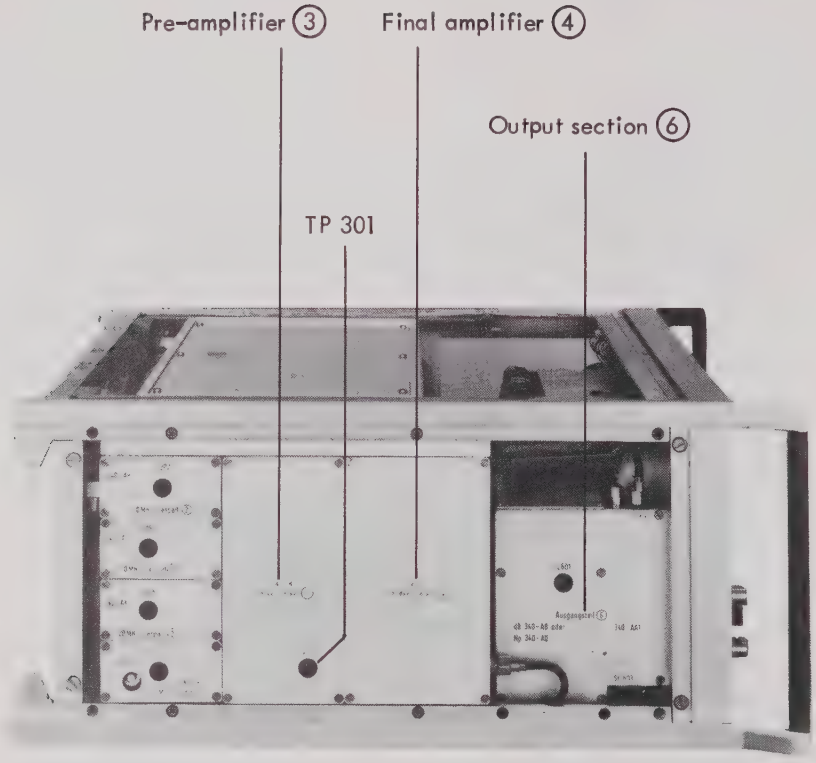


Fig. 7-4 Left view

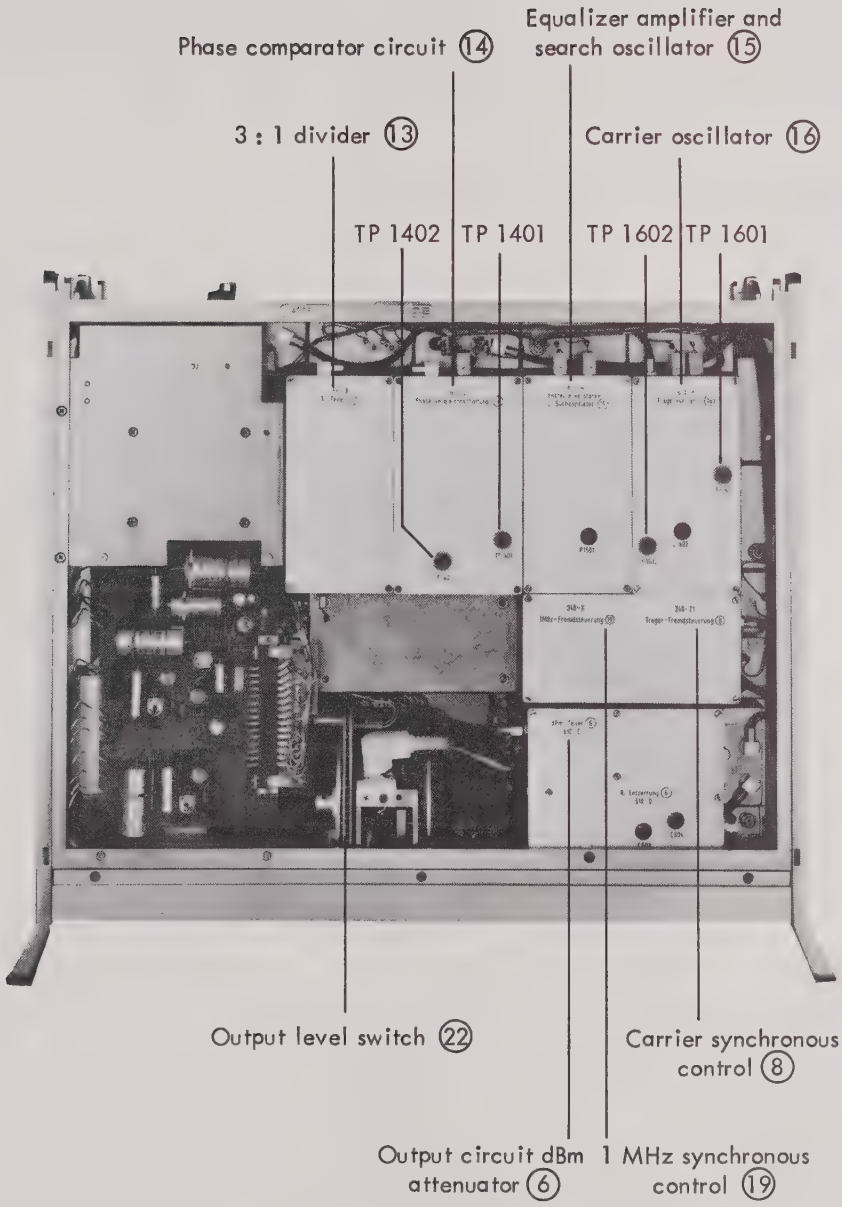


Fig. 7-5 Bottom view

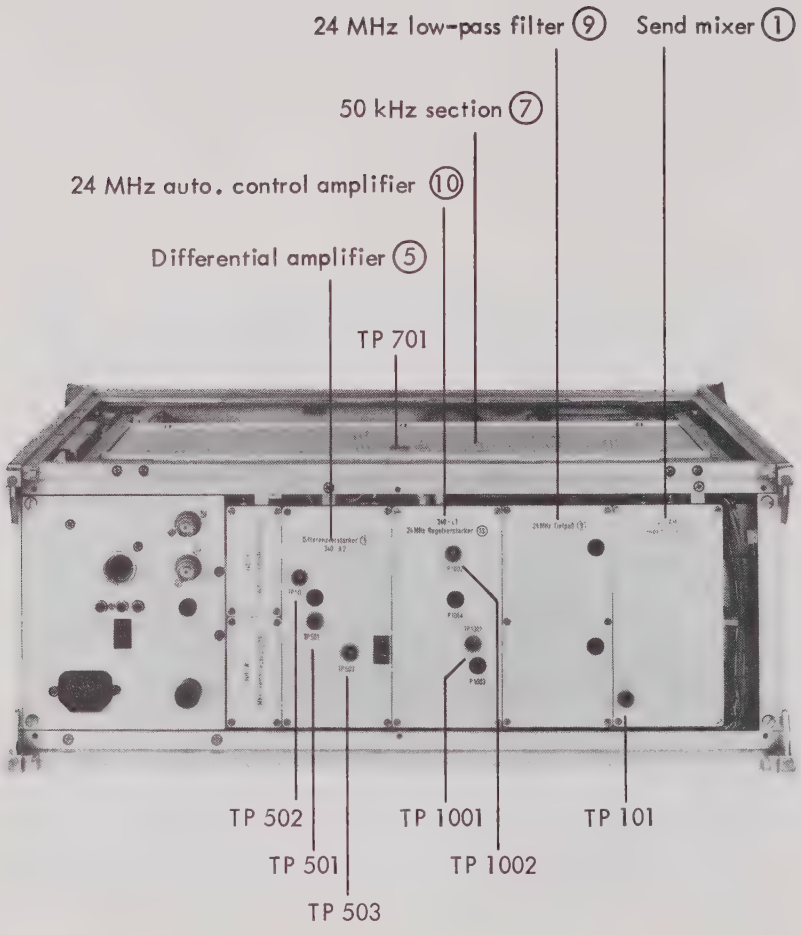


Fig. 7-6 Rear view

7. FAULT LOCALIZATION AND REPAIR INSTRUCTIONS

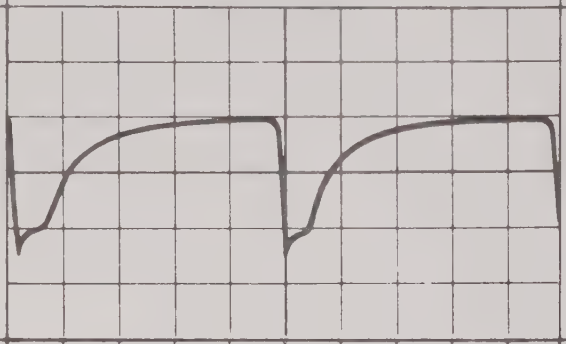
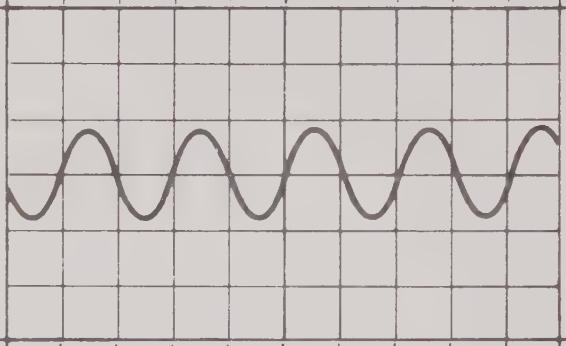
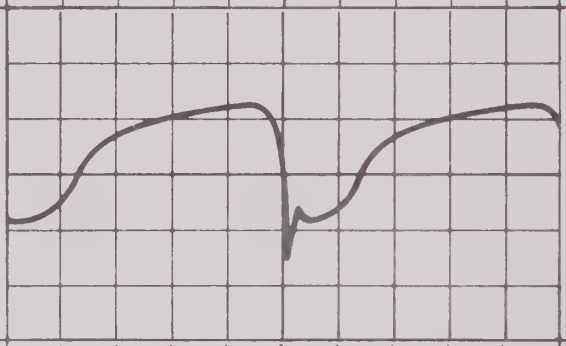
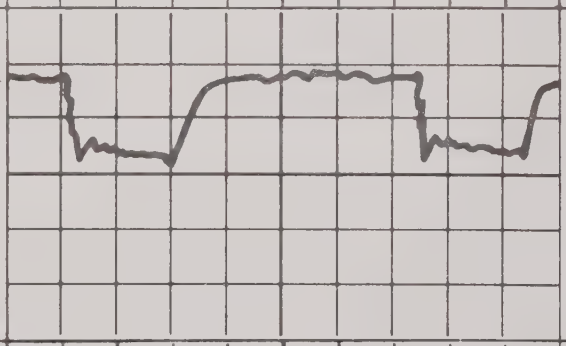
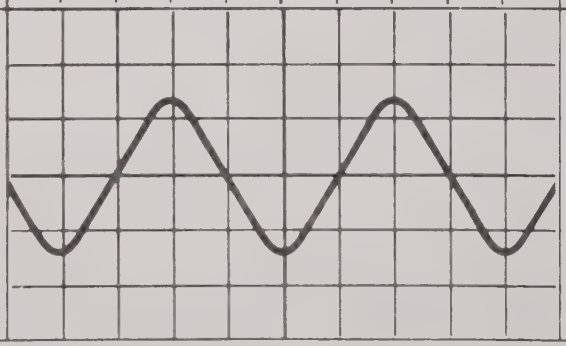
Test point	Frequency	Nominal value Level reading in dB, 0 dB = 0.75 V	Measured with	Notes
TP 101	24 MHz	-19 dB	PSM-5+TK-8	when modulation connector Bu 1001 a [1] is used; Nominal level: - 25 dB
TP 301	100 kHz	-46 dB	PSM-5+TK-8	when modulation connector Bu 1001 a [1] is used; Nominal level: - 52 dB
TP 401	D.C.	-7 V	100 kΩ/V	Measurement possible only after removal of cover
TP 501/502	D.C.	±30 mV	100 kΩ/V	when stabilizer is opened approx. ± 1 V
TP 503	D.C.	+1.1 V	100 kΩ/V	With blanking approx. + 10 V, when stabilizer loop is opened, approx. ± 10 V
Output II Bu 604	100 kHz	-10 dB	PSM-5+TK-8	When modulation connector [1] is used Nominal level: - 16 dB
TP 701	50 kHz	+6 dB	PSM-5+TK-8	Voltages occasionally checked: $U_{operating}$ = 12 V ± 0.1 V
TP 1001	24 MHz	-17 dB	PSM-5+TK-8	Level remains the same when mod. connector [1] is in use
TP 1002	24 MHz	-18.5 dB	PSM-5+TK-8	when mod. connector is in use [1], Nominal level: - 24.5 dB
TP 1401	D.C.	-200 mV to +200 mV	100 kΩ/V	when the auto. control loop is not locked (13) (14) (15) (16), the search oscillator (16) must oscillate
TP 1601	D.C.	+10 V at f = 24 MHz	100 kΩ/V	If (16) [2] is verified, then the checks at (13) (14) (15) can be eliminated
TP 1801	D.C.	approx. +8.3 V (6.5 to 10.5 V)	100 kΩ/V	0.2 V below the mean auto. control voltage
TP 2401	D.C.	+12 V	100 kΩ/V	when blanked, - 6 V
Point R (25)	D.C.	+ 180 V	100 kΩ/V	Voltage measured to chassis-ground
Points 1 to 8 (25)	D.C.	+ 12 V ± 0.05 V	100 kΩ/V	Voltage measured to chassis-ground
Point 5 (25)	D.C.	- 14.4 V	100 kΩ/V	Voltage measured to chassis-ground
Points a to f (25)	D.C.	- 12 V ± 0.05 V	100 kΩ/V	Voltage measured to chassis-ground
Points 9 to 12 (25)	D.C.	+ 5 V	100 kΩ/V	Voltage measured to chassis-ground

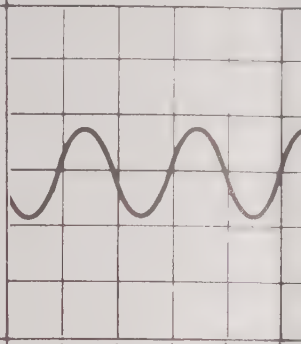
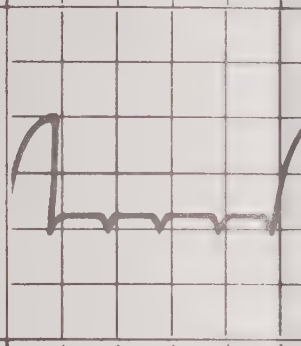
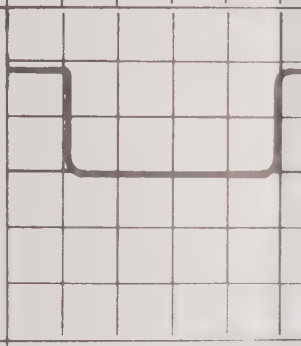
PS-60/BN 610
Level Plan

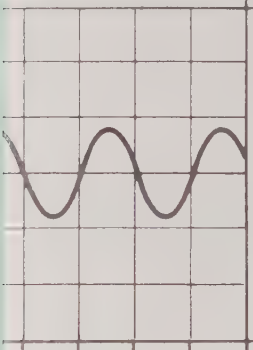
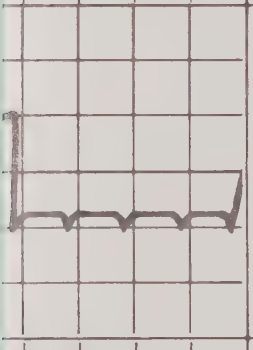
Notes:

1) The levels at these test points are mean values. Deviations which might be observed from test point to test point are corrected by the auto. level control and do not affect the send level. Through use of the modulation connector with switch (Bu 1001 a) located on the back panel of the PS-60, the differential amplifier is switched to a fixed operating point. With that the auto. level control loop is opened, and the 50 kHz reference voltage is switched off.

2) In order to correlate with all the carrier oscillator operating points, the complete frequency range must be turned through from d.c. to 18.6 MHz. If an a.c. voltage appears at the test points, then the oscillator is no longer locked to the standard frequency. FAULT.

Test point	Oscillogram	Data
TP 1101 f= 1.000 MHz		5 V/cm 0.2 µs/cm
TP 1102 f= 1.000 MHz		1 V/cm 0.5 µs/cm
TP 1103 f= 1.000 MHz		0.5 V/cm 0.2 µs/cm
TP 1402 3:1 divider		2 V/cm 20 µs/cm
TP 1601 f= 24.000 MHz		0.5 V/cm 1 µs/cm

Test point	Oscillo
TP 1802 f= 24.000 MHz	
TP 2001 f=200 kHz	
Bu 2102 f=10 kHz	

ram	Data
	0.5 V/cm 0.04 µs/cm
	5 V/cm 1 µs/cm
	5 V/cm 20 µs/cm

Test point	Oscillogram	Data

8. CHECKING OF IMPORTANT TECHNICAL SPECIFICATIONS

In the following, procedures are described for checking the most important specifications of the PS-60. According to usage, normally available test instruments are suggested.

If not otherwise stated, testing should be done at room temperature (+23°C ± 3°C).

Because the specified values are valid immediately after the PS-60 is switched ON, the suggested measurements do not require any warm-up time.

Verifying the most important specifications should determine whether the indication of a measuring quantity lies within the guaranteed accuracy limits. Verification is only successful without qualifications or restrictions when the self-introduced error of the applied measuring configuration can be neglected.

Otherwise, the following rules are valid:

If the applied measuring configuration has an error ± m, and if the guaranteed error limits for the test specimen are stated as ± e, then

> a violation of the limits ± (e+m) indicates that the guaranteed error limits have been surely violated, staying within the limits ± (e-m) indicates that the guaranteed error limits have been surely maintained.

In all measuring regulations, the value of "e" is stated. The value "m" is directed towards the particular measuring instrument, and for that reason generally must be determined from case to case. The measuring regulations only state the value "m" when the prescribed measuring materials are not permitted to have any variation or if special condition must be observed.

With a systematic verification of specifications, there should be adherence to the hereby given sequence of tests.

First, the test specimen should be lined-up after determining if the limit ± (e + m) has been violated.

8.1. Frequency readout

Required test-instruments:
1 Frequency counter, e.g. FZ-4 from W&G

Measuring configuration:

Fig. 8-1

Adjusting the instruments
PS-60: f = 10 MHz, 0 dB, Z_{out} = 0

FZ-4: f/kHz, measuring time 1 s

Adjust 10 MHz at the PS-60. For vernier tuning, pull out tuning knob (FINE) and depress push button S 2101.

Read frequency on FZ-4.

Error limit (e) of the frequency readout at 10 MHz:

$10 \times 10^6 \times (\pm 4 \times 10^{-6} \pm 1 \text{ unit}) = \pm 50$ Hz

8.2. Send level 0 dB or 0 dBm (f = 6 kHz to 18.6 MHz)

Required test instruments:
1 Milliwatt Test Set, e.g. EPM-1 from W&G
with accessory attenuation network 9.03 dB
Z_o = 75 Ω

Measuring configuration:

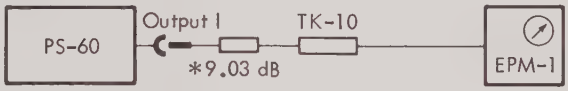


Fig. 8-2

*Attenuation network is not used at 0 dBm measurement. Attenuator or Test Probe directly connected to output of PS-60, if possible without connecting cable.

Adjusting the instruments:
PS-60: 0 dB or 0 dBm, Z_{out} = 75 Ω, scale range: 2 dB, meter zero point has been adjusted.

EPM-1: for the 0 dB measurement
calibrated with attenuator 9.03 dB at calibration level 0 dB, Z_{out} = 75 Ω
for the 0 dBm measurement
calibrated without attenuator network at calibration level 0 dBm, Z_{out} = 75 Ω

Measuring conditions: + 20°C ambient temperature

PS-60 frequency varied over complete range (6 kHz to 18.6 MHz) and read EPM-1 for send level deviation compared to 0 dB or 0 dBm.

Error limit (e) of send level:

f = 20 kHz to 6 MHz: ± 0.15 dB
f = 6 kHz to 18.6 MHz: ± 0.20 dB

With the ambient temperature deviating from the nominal value (+20°C) the send level temperature coefficient, ± 0.01 dB/°C should be taken into account.

8.3. Error of the send level switch

Required test instruments:
1 Selective Level Meter, e.g. SPM-60 from W&G
1 Calibrated attenuator 0 to - 80 dB, Z_o = 75 Ω
e.g. Siemens Rel 3 D 120

Measuring configuration see Fig. 8-3.

Adjusting the instruments:

PS-60: Synchronous tuning of SPM-60, 0 dB, Z_{out} = 75 Ω

8. CHECKING OF IMPORTANT TECHNICAL SPECIFICATIONS

SPM-60: -78 dB, f = 6 kHz, Z_{in} = 75 Ω, bandwidth 1.74 kHz, scale range ±0.5 dB, SLOW reading
Calibrated attenuator: 78 dB attenuation

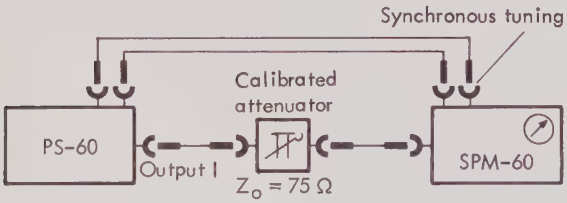


Fig. 8-3

At the selected settings, the SPM-60 reading should be set at exactly 0 dB.

PS-60 level decreased in steps with send level switch and correspondingly reduce the attenuation of the calibrated attenuator. Read error at SPM-60.

Verify following steps:

Measuring frequencies of 6 kHz, 20 kHz, 6 MHz, 18.6 MHz

0 to - 10 dB	in steps of 2 dB each
- 10 dB to - 70 dB	in steps of 10 dB each
- 78 dB	end setting of send level switch

Error limit (e) of send level switch referred to setting 0 dB:

f = 20 kHz to 6 MHz: ± 0.10 dB
f = 6 kHz to 18.6 MHz: ± 0.20 dB

8.4. Meter Scale Division Error

Required test instruments and measuring configuration as in 8.3.

Adjusting the instruments:

PS-60: Synchronous tuning by SPM-60, 0 dB, Z_{out} = 75 Ω
SPM-60: - 20 dB, f = 20 kHz, Z_{in} = 75 Ω, bandwidth 1.74 kHz, scale range ±0.5 dB, SLOW reading

Calibrated attenuator: 20 dB attenuation

8.4.1. Meter scales, + 1 dB to - 20 dB

At the selected settings, the PS-60 and SPM-60 readings should be set at exactly 0 dB.

Corresponding to the following table, adjust level at the PS-60, select attenuation at calibrated attenuator and read level error on meter of SPM-60.

Scale division mark	Calibrated attenuator	error limit (e)* of meter scale
0 dB	20 dB	reference point
+ 1 dB	21 dB	± 0.08 dB
- 5 dB	15 dB	± 0.15 dB
- 10 dB	10 dB	± 0.25 dB
- 14 dB	6 dB	± 0.40 dB
- 20 dB	0 dB	± 0.80 dB

Table 8-1

*The error given in dB corresponds to 1 % f.s.d. at the relevant scale mark.

8.4.2. Meter scales, + 0.3 dB to – 2.2 dB

At the selected settings, the PS-60 and the SPM-60 readings should be set at exactly 0 dB. Corresponding to the following table, adjust level at PS-60, select attenuation at calibrated attenuator and read level error on meter of SPM-60.

Scale division mark	Calibrated attenuator	Error limit (e) of meter scale
0 dB	20 dB	reference point
+ 0.3 dB	20.3 dB	± 0.03 dB
- 0.5 dB	19.5 dB	± 0.03 dB
- 1.0 dB	19 dB	± 0.03 dB
- 1.5 dB	18.5 dB	± 0.03 dB
- 2.0 dB	18 dB	± 0.03 dB

Table 8-2

8.5. Harmonic ratio of send level

Required test instruments:
1 Selective Level Meter, e.g. PMO-5 from W&G

Measuring configuration:

Fig. 8-4

Adjusting the instruments:

PS-60: 0 dB, Z_{out} = 75 Ω
PMO-5: Z_{in} = 75 Ω, measurement mode "low distortion", bandwidth 500 Hz

Reference point is the level reading on the PMO-5 at the fundamental frequency. Then, tune to the harmonics, k_2 or k_3, and read the level (≅ harmonic distortion or harmonic ratio)

8. CHECKING OF IMPORTANT TECHNICAL SPECIFICATIONS

The PMO-5 sensitivity should not be raised by more than 50 dB.

Error limit (e)

Harmonic ratio k_2 and k_3 for fundamental

6 kHz: 40 dB
20 kHz: 50 dB
6 MHz: 50 dB
18 MHz:40 dB

Note:
Because the upper frequency limit of the PMO-5 is at 36 MHz, only k_2 can be measured at 18 MHz. This measurement is sufficient owing to harmonic ratio k_3 (54 MHz) not being expected to be excessive.

8.6. Return loss coefficient at output I

Required test instruments:
1 Return loss coefficient measuring bridge, e.g. RFZ-5 from W&G
1 Level Generator and Level Meter for driving the measuring bridge, e.g. PSM-5 from W&G

Measuring configuration:

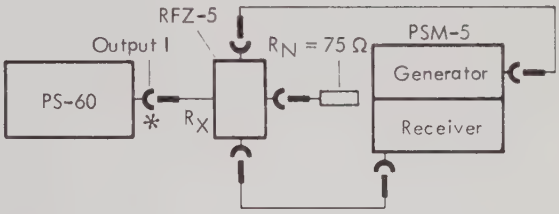


Fig. 8-5

*Return loss coefficient measuring bridge directly connected to output of PS-60, if possible without connecting cable.

Adjusting the instruments:

PS-60: - 78 dB, f approx. 100 kHz, Z_{out} = 75 Ω
PS-5: approx. - 2 dB, Z_{out} = 75 Ω
PM-5: Z_o = 75 Ω, low noise, bandwidth 500 Hz
RFZ-5: calibrated in conjunction with PSM-5 and return loss standard r = 0.1 (≙ 20 dB return loss)

The return loss factor measurements are done at 1 MHz, 16 MHz and 18.6 MHz (frequency settings PSM-5)

Error limit (e)
Return loss factor r = 0.02
(this value corresponds to a return loss of 34 dB)

9. ALIGNMENT INSTRUCTIONS

If the PS-60 does not function perfectly or if the specified values deviate from the guaranteed specifications, then this chapter provides information about the required alignment and adjustment measures to be taken. With that, at the same time Chapter 8 "Checking of Important Technical Specifications" should be observed.

9.1. 1 MHz Oscillator (11) frequency alignment

Required test instruments:

1 Frequency counter	e.g. Grundig FZ-74
1 Test Probe	e.g. Grundig TK-5
1 Multimeter 100 kΩ/V	e.g. AEG
1 Oscilloscope with probe	e.g. Tektronix
1 Level Measuring Setup	e.g. PSM-5 from W&G
1 Digital voltmeter 3 1/2 digits	e.g. HB

The frequency is measured at TP 1102, frequency is trimmed with C 1102. Nominal value: 1 MHz ± 2 Hz

Because the frequency of the 1 MHz oscillator is exactly adjusted within approx. ± 1 Hz at the factory, it is unrealistic to attempt measurements to that accuracy with the usually available frequency meters of the type suggested above which have large self-introduced errors. The guaranteed accuracy of the SPM-60 is however assured if the uncertainty of 1 MHz frequency ± 10 Hz is not violated.

If a sufficiently accurate 1 MHz frequency standard is available, then the measurements also can be made through using Lissajous figures presented on an oscilloscope screen.

Voltage peaking is done at Ü 1101 so that maximum voltage is present at TP 1102.
Nominal value: ≧ 1.2 V_{p-p}.

9.2. Adjusting the frequency and tracking range of the 24 MHz oscillator (18)

The frequency may be measured at TP 1802, the A.F.C. voltage at TP 1801. The variation range of the A.F.C. voltage is determined through rotating the aligning screw in L 1803. The limits of this variation range are located at the frequencies where the 24 MHz oscillator no longer locks in. For this reason the aligning screw is to be adjusted so that the voltage at TP 1801 is about 0.2 V below the mean value of A.F.C. voltage. Nominal value: approx. 8.3 V.

9.2.1. Measuring the tracking range

With this, the 1 MHz oscillator (11) is caused to be inoperative in that e.g. the crystal holder is removed from its socket: A suitable Generator (e.g. the PSM-5 from W&G) feeds a signal, 1 MHz at 0 dB, to test point TP 1102. Then, this applied synchronizing frequency is varied, and the frequency counter is observed to see the range over which the synchronizing frequency can be varied within the tracking range of the A.F.C. Referred to the 1 MHz synchronizing frequency, the tracking range is:

24-MHz-oscillator (18) $\Delta f \geq \pm 7$ kHz

9.3. Alignment of 50 kHz oscillator (7)

The oscilloscope test probe is connected to terminal 5 on transformer Ü 701. At this point, the voltage should be about 7 V, see Fig. 9-1.

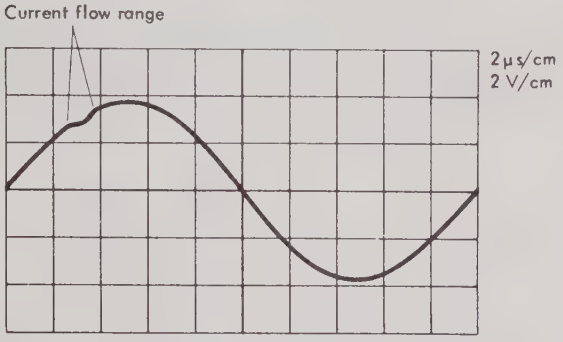


Fig. 9-1

Frequency alignment may be done either with the aid of a Lissajous figure on an oscilloscope or with a frequency counter.

Nominal frequency 50 kHz. The alignment results from rotating the core of Ü 701.

If the frequency deviation is ≦ ± 1 % (≙ 500 Hz), then alignment is not necessary.

9.3.1. Circuit alignment L 701/C712

The selective level meter is connected via the test probe to TP 701 (50 kHz). Switch 701 is set to "20 dB" potentiometer P 703 (Level adjustment) is used to set the measured level to be + 6 dB. However, if this level is not achieved, then P 702 should be accordingly readjusted. Thereafter, readjust coil core of L 701 until the indication reaches a maximum.

9.3.2. Adjusting the level range

Set potentionmeter P 703 to the right stop (= maximum level) and adjust P 702 to set level at + 8 dB on level meter.

Then P 703 is rotated to the left stop, and with P 701 the level is adjusted to - 21 dB on level meter. Alternately use P 702 and P 701 for alignment as long as necessary until the deviation remains within the following limits:

for P 702	+ 8 dB ± 0.2 dB
for P 701	- 20.5 dB to - 21.5 dB

If the 50 kHz oscillator and the level range are newly

9. ALIGNMENT INSTRUCTIONS

aligned, then additionally repeated must be calibrating the absolute level and the reading (para. 9.6.).

9.4. Alignment of auto.control amplifier

Dertermining the auto. control voltage

Apply a floating voltage of + 300 mV between points 8 and 9 of the auto. control amplifier (see Fig. 9-2). The connection must be opened from point 8 to the differential amplifier.

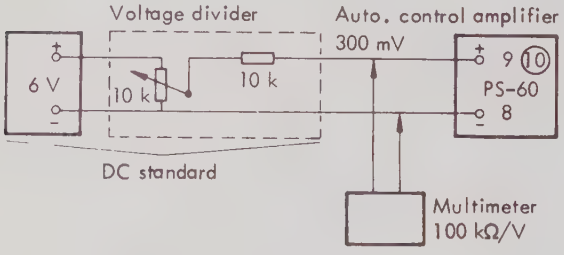


Fig. 9-2

Read level at TP 101 with Level Meter PSM-5. Reduce level by 6 dB at TP 101: change DC voltage between points 8 and 9. If necessary, the voltage polarity must be reversed. Now, note the value of d.c. (sign must be correctly referred to point 8 !)

Adjust the auto. control voltage

Take voltage away from points 8 and 9, and again close connection to point 8. DC voltmeter or digital voltmeter across points 8 and 9, and adjust potentiometer P 1003 so that the auto. control voltage is equal to or near the value previously noted (observe polarity).

9.5. Changing diodes GI 601 and GI 602 (output circuit (6))

Because the difference in characteristics between the two diodes used in the peak value rectifier is not included in the automatically controlled level available at the PS-60 output, these two diodes must be specially matched as a pair. Therefore, when required, the pair of diodes should be ordered from W&G.

Changing diodes is accomplished as follows:
After removal of the left side panel, the cover marked "output section 6" (Ausgangsteil 6) is unscrewed. Now, diodes GI 601 and GI 602 can be unsoldered. Bend the leads of the new diode pair according to the leads of the removed pair. Thereafter, the following alignment is to be done:

Adjust output level switch to - 8 dB (voltage level), switch S 701 to 2 dB and meter reading at 0 dB on J 701. Additionally, Level Generator PS-60 must be set at 50 kHz.

With the Level Meter of Level Measuring Setup PSM-5 and a Scale Expander, measure selectively over the Test Probe the 50 kHz level at point 4 of printed circuit board 340 - AA1. Thereafter, apply the Test Probe to point 3 of the same printed circuit board, and as well measure the 50 kHz level. This level reading is adjusted by means of rotating potentiometer P 501 in the differential amplifier so that it measures the same as that measured at point 4.

The resolution of the applied Level Meter must be so good that levels can be balanced to a difference of ≦ 0.02 dB.

Caution: Because under certain conditions, the two frequencies might not be identical at the two test points, the selective Level Meter must be retuned for every measurement. In addition, every change of diodes must be concluded with alignment of the auto. control amplifier (10) (according to para. 9.4.) as well as of the absolute level (para. 9.6.).

9.6. Aligning the absolute level and the meter reading

Required test instruments:
1 Milliwatt Test Set, e.g. EPM-1 from W&G
with accessory attenuation network 9.03 dB
$Z_o = 75\ \Omega$

Measuring configuration:

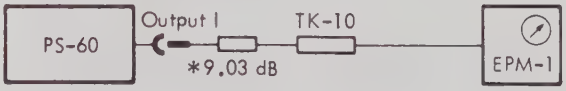


Fig. 9-3

*Attenuation network is not used at 0 dBm measurement. Attenuator or Test Probe directly connected to output of PS-60, if possible without connecting cable.

Adjusting the instruments:
PS-60: 0 dB or 0 dBm, $Z_{out} = 75\ \Omega$, scale range 2 dB, meter zero point has been adjusted.

EPM-1: for the 0 dB measurement
calibrated with attenuator 9.03 dB at calibration level 0 dB, $Z_{out} = 75\ \Omega$
for the 0 dBm measurement
calibrated without attenuator network at calibration level 0 dBm, $Z_{out} = 75\ \Omega$

9. ALIGNMENT INSTRUCTIONS

Measuring conditions:
+ 20°C ambient temperature

Alignment of absolute level:

The alignment is accomplished at a send frequency of f_s = 20 kHz, and output impedance of the PS-60 at Z_{out} = 75 Ω and 20 dB send level. Switch S 701 is set at 20 dB.

Potentiometer P 703 (front panel) is then adjusted so that through comparison with the meter of EPM-1 PS-60 output level is at 0 dB absolute. Thereafter switch S 701 is switched to 2 dB on the PS-60 and with potentiometer P 704 in the 50 kHz section (7) the adjustment is made for 0 dB absolute (with that, the cover of the hinged chassis must be removed).

Alignment of the meter reading:

Switch S 701 is again switched to 20 dB and with potentiometer P 706, the PS-60 reading is set at 0 dB. Thereafter, rotate switch S 701 to 2 dB and P 705 is used to cause a 0 dB reading.

This alignment is to be repeated until the PS-60 reading is identical with the measured absolute level.

9.7. Harmonic distortion alignment (pre-amplifier and final amplifier (3) (4)

Measuring configuration:

$Z_{out} = Z_o = 75\ \Omega$ $Z_{in} = Z_o = 75\ \Omega$

Fig. 9-4

Alignment of the pre-amplifier:

The send level is set to be 0 dB, the send frequency is at 3 MHz. Then the PMO-5 (selective level meter) is used to measure the harmonic distortion aK_2, and potentiometer P 302 is adjusted for the best possible value. Nominal value $aK_2 \geq 51$ dB.

Alignment of the final amplifier:

The PS-60 Generator is set at fs = 6 kHz and 0 dB, additionally potentiometer P 403 is used to set - 7 V at TP 401. This measurement should be made with a multimeter, 100 kΩ/V, in the 30 V range. In addition, potentiometer P 402 is used to adjust the quiescient current in the end transistors so that 35 mA flows through R 440. Repeat alignment.

Analogous to that, the PS-60 is set at 12 MHz and the selective Level Meter (e.g. PMO-5) is set to 24 MHz. A send level of 0 dB is used with P 401 to adjust for minimum harmonic distortion aK_2.
Check nominal values:

at the fundamental frequency fs = 6 kHz $aK_2 \geq 41$ dB
at the fundamental frequency fs = 12 MHz $aK_2 \geq 51$ dB

After this alignment procedure, the auto. control voltage should be checked at the auto. level control amplifier (see para. 9.4.) and accordingly readjusted.

9.8. Modulation : adjusting the operating point (10)

Measuring configuration:

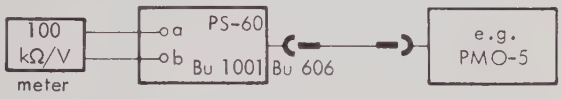


Fig. 9-5

The send level is adjusted to 0 dB, the send frequency fs to 100 kHz and the multimeter is connected to contacts a and b of Bu 1001. Then potentiometer P 1002 is to be adjusted until the multimeter reads 0 (scale : 60 mV). Potentiometer P 1001 is used to adjust the output level to be - 6 dB (with connector Bu 1001 in use, this output level can be read only on the Level Meter!). Additionally P 1002 is to be again adjusted until the multimeter reads 0. Thereafter, repeat the alignment.

9.9. Carrier generation (16) (adjusting the operating point)

The PS-60 is set to the send frequency fs = 0 Hz and the counter reading is verified. Plug jumper a - b in equalizer (15). Point 1 (13) (input 3:1 divider short circuited to chassis-ground (keep connection length short!) and adjust potentiometer P 1501 for V = + 1 V at TP 1602.
Therafter, remove a - b. Use oscilloscope at TP 1602 to view search oscillator frequency. (auto. control loop (13) (14) (15) (16) not locked-in).

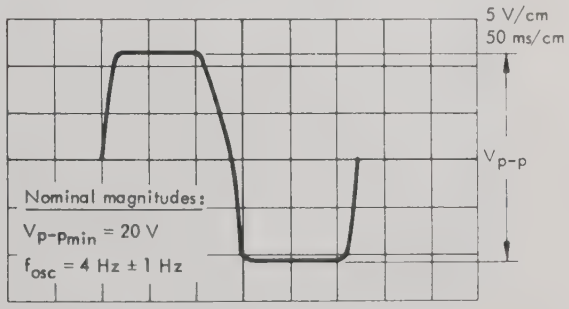


Fig. 9-6 Oscillator 1: search oscillator frequency (f_{osc}, approx. 4 Hz)

9. ALIGNMENT INSTRUCTIONS

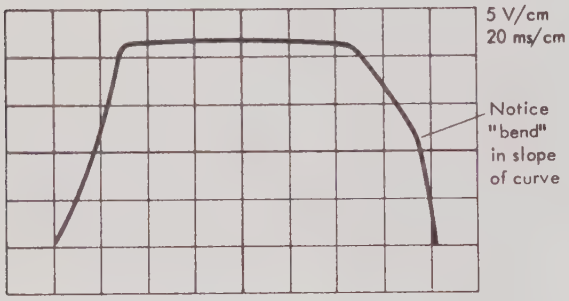


Fig. 9-7 Specimen of search oscillator signal

Remove short circuit at point 1 (13) and turn core of coil L 1602 (carrier oscillator) to align so that at TP 1602, there is V = + 10 V.

Then set the PS-60 to the send frequency f_s = 18.6 MHz and read voltage at TP 1602. $V_{nominal}$ = - 10 V.

Additionally, with an oscilloscope check the sinusoidal output voltage of the carrier oscillator at TP 1601. Nominal magnitudes: $V_a \geqq 0.45\ V_p$, Typical $V_a = 0.6\ V_p$.

The output voltage should be sinusoidal and not have any parasitic oscillations superimposed on it.

9.10. Power supply voltage + 5 V (25)

First measure V_b with a digital voltmeter at C 1309. Thereafter adjust potentiometer P 2503 so that the counter, C 2129 is at V_b = + 4.8 + 0.05 V.

10. DESCRIPTION OF FUNCTION

10.1. Complete instrument

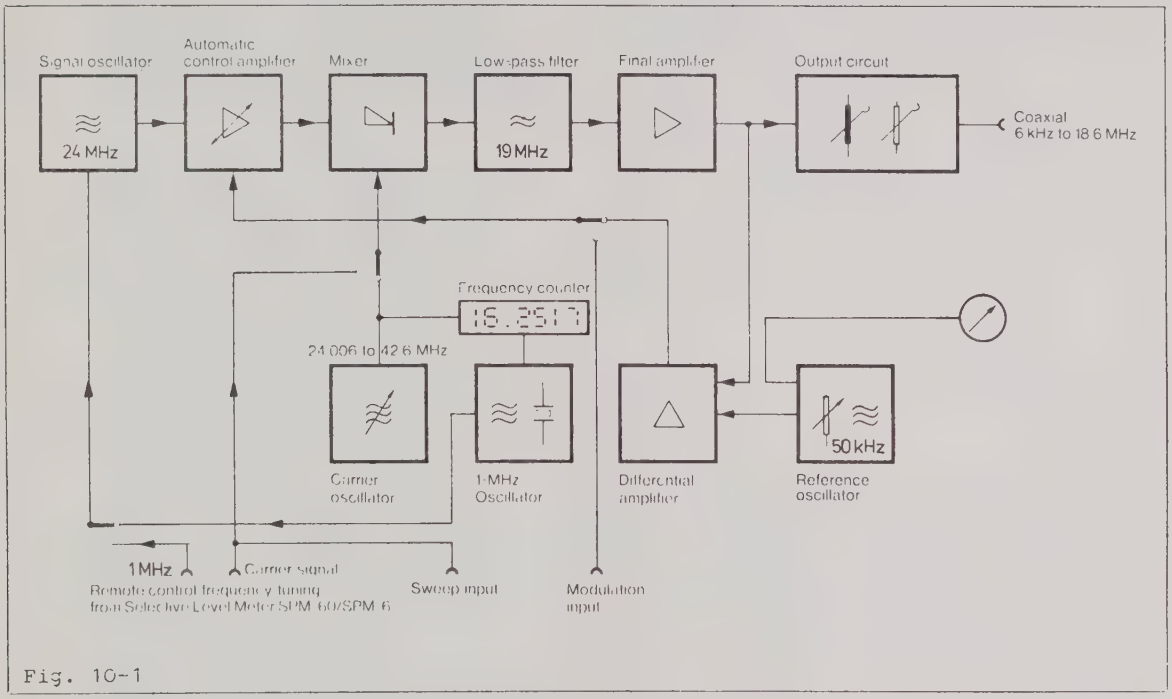


Fig. 10-1

The PS-60 differs in the principle characteristic data not at all or only slightly from the PS-6 and is only apparent by virtue of its modified exterior. The following properties should be mentioned:

The frequency range extends from 6 kHz to 18.6 MHz, whereby the transmission frequency set is indicated by a counter. The level range of the PS-60 is adjustable in 2 dB stages from 0 to -78 dB whereby the output level is kept constant by internal regulation before the 10 dB coarse stages of the output divider. In addition the level adjustment can be carried out on voltage or power level.

The facility for "Soft" keying off of the transmitter, the modulation and the external control combine with the sweepability through the WZ-6 complete and extend the range of application of the instrument. In the paragraphs below further details will be given of the properties mentioned.

10.1.1. Frequency generation

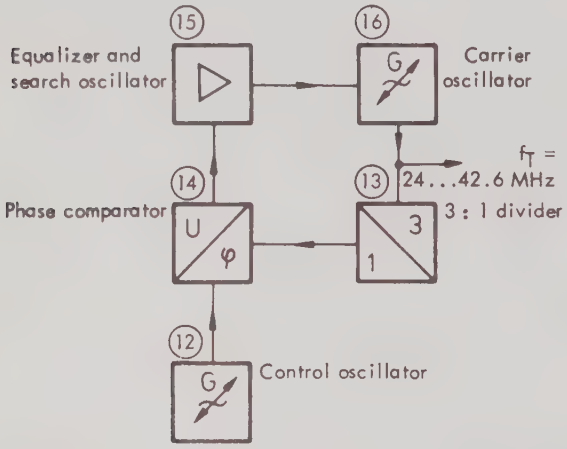
The output frequency of 6 kHz to 18.6 MHz is formed with the aid of the carrier frequency variable in the range from 24.006 MHz to 42.6 MHz in the transmission mixer (1) in combination with the 24 MHz signal frequency (18). After suitable filtering in the 20 MHz low-pass filter (2) as well as amplification in the pre- and output amplifier (3) and (4), the signal passes through the output circuit (6) to the output.

The 24 MHz signal frequency is derived from a 1 MHz crystal oscillator (11) and thus has the same accuracy as this oscillator. "Tying" the intermediate oscillator to the crystal oscillator is effected as follows:

The output voltage of an LC oscillator which oscillates at the desired frequency is compared with the signal of the 1 MHz oscillator in a sampling phase meter and the DC voltage obtained from the phase difference of the two oscillations is used to correct the LC-oscillator. On operating the transmitter blanking (S 2401) the supply voltage for the 24 MHz oscillator and the pulse shaper is interrupted.

The carrier frequency for the transmission mixer (1) is also generated in a control circuit:

10. DESCRIPTION OF FUNCTION



Block circuit diagram:10-2

The carrier frequency of 24 MHz to 42.6 MHz occurs as a result of tripling the control frequency of 8 MHz to 14.2 MHz. The tripling takes place with a phase control circuit whose command variable is formed by the control oscillator. For this purpose the carrier frequency is divided in the ratio of 3:1 and compared with the control frequency in the phase comparator.

The output voltage of the phase comparator is proportionate to the phase difference of the input frequencies. In engaged state (the control circuit is operative) the output voltage is a DC voltage of definite magnitude, in unengaged state the difference frequency of the input frequencies occurs. An RC low pass filter at the output of the phase comparator corrects the frequency response of the control loop. With this correction stable operation of the control loop is ensured.

The equalizer has two functions:

a) Matching the output voltage of the phase comparator to the capacitance diode characteristic in the carrier oscillator (characteristic bend amplifier).

b) Assisting the capture process of the control loop in oscillator connection. (Search oscillator as starting aid when the instrument is switched on.)

Re.a) The voltage-frequency characteristic (slope) of the carrier oscillator is not linear.

For considerations of stability however linear transient behaviour is required.

By means of voltage-dependent negative feedback of the amplifier the static transient behaviour of the control circuit is linearized to a large extent. Gain is designed so that the maximum possible voltage range is available at the output of the amplifier.

Re.b) The RC low pass filter narrows the capture range of the control circuit. To permit positive capture at all times the capture range must be extended. A search oscillator assumes this function and pre-oscillates with the control loop in unengaged state. Now the useful range of the carrier oscillator characteristic is run through with an oscillation frequency of 4 Hz. On reaching the control frequency the control loop engages and search oscillation is terminated.

The 1 MHz crystal oscillator is additionally used as time base for the counter (21). Then its output signal is divided in the frequency divider (20) and passed to the counter as 10 kHz pulse sequence. As the transmission frequency of the PS-60 is determined directly by the carrier frequency and the latter in turn is linked in locked phase relation to the frequency of the control oscillator (12), for measurement of the transmission frequency the lower frequency of the control oscillator is used. Its frequency can also be fine tuned by means of an additional adjuster on the front panel.

10.1.2. External control by SPM-60, SPM-6

If transmitter and receiver are used on the same location the transmission frequency can be determined synchronously from the receiver. In the case of external control operation the external control switch S 802 in the PS-60 should be switched to "SPM-6, SPM-60" position. In addition two auxiliary connections should be established with the receiver. synchronism is thus established without any matching as both the carrier and the 1 MHz standard frequency are taken over by the controlling instrument.

In the transmitter, as already described, the signal frequency of 24 MHz is derived from the 1 MHz frequency. The "1 MHz external control circuit" (19) in the PS-60 incorporates an isolating transformer and a buffer stage. If the external control switch S 802 is moved to "SPM-6, SPM-60" position, the buffer stage in circuit (19) receives its supply voltage and in addition an

10. DESCRIPTION OF FUNCTION

output stage in the SPM-60 receives its current supply through the external control line. In order to prevent cross talk in all cases the circuits of the carrier frequency generator in the PS-60 which are not required are switched off. The circuits concerned can be seen in the block circuit diagram.

The carrier frequency of 24 to 42.6 MHz passes through the 2nd connection from the receiver to the transmitter (Bu 801). Through a buffer stage in circuit (8) and a further buffer stage in the carrier oscillator (16) the carrier frequency passes to the transmission mixer.

The external control switch S 801 in position 1 (ON) establishes contact of Bu 801 with the buffer stage through a relay contact and switches on the power supply for the buffer stage in circuit (8). With S 801 (OFF) a relay contact (in circuit (8)) applies the carrier voltage from the SPM-60 to chassis. By this means it is possible to plug the external control connections with separate operation without interference occurring as a result of cross talk of the external control signals.

10.1.3. Level indication and level control

A control circuit at the output of the output amplifier or at the input of the output divider chain generates a constant level. At this point a peak rectifier intercedes which supplies a DC voltage proportionate to the level and frequency independent. A 2nd peak rectifier receives a 50 kHz voltage which acts as reference voltage for the output level. The difference voltage from the 2 rectifier circuits is amplified in the differential amplifier (5) and passed to the control amplifier (10).

The control amplifier now varies the signal voltage (24 MHz) so that at the output of the output amplifier a level of the magnitude of the 50 kHz reference voltage occurs.

Varying the reference voltage always produces a change in the transmission level. For this reason the reference voltage is used for the transmission level display (I 701) and for transmission level adjustment in four 2 dB stages with Ü 703 and continuously by 20 dB with P 703. In addition level matching at power level is made possible by means of Ü 608.

This type of control circuit compensates frequency responses in the transmission mixer (1), 20 MHz low pass filter (2) preamplifier (3) and output amplifier (4) modules. With adequate control slope only the frequency response of the rectifier circuit itself occurs at the connection point of the rectifier circuit. Peak rectification has been chosen as this is best as regards frequency response error.

The following points could be named as disadvantages of the control circuit.

The distortion at the output of the output amplifier can produce a level change on account of the distortion sensitive peak rectifier.

When altering the 50 kHz reference voltage for transmission level adjustment level errors of the transmission level may occur if the two rectifier circuits have characteristic differences.

On failure of the transmission level J 701 always supplies the same indication as long as the 50 kHz section remains in tact. In order to eliminate this error an auxiliary circuit has been incorporated which shuts off the display (I 701) in the case of overload of the differential amplifier. As a result the user is warned when the control circuit is out of operation and the transmission level is not correct.

The display circuit in the 50 kHz section also permits switching on an extended display range. The scope of display in this range is 2.5 dB. As a result of the pronounced extension the scale graduation is practically linear. In order to obtain as linear rectification as possible in the unextended range as well (+1 to -20 dB), average response rectification has been chosen here. There are no frequency response requirements in the case of this circuit.

10.1.4. Output circuit

The output circuit incorporates the rectifier circuits already mentioned for level control and the power level transformer. Between the supply point at which the level is kept constant and output I, are located the divider transformers, the equalizers for frequency response and the reflection factor, as well as selection for the internal resistances R_i = 0 and R_i = 75 Ohm.

By combination of the various divider transformers attenuation of 0 to 70dB can be introduced in 10 dB stages. The combination in question is determined by the output level switch (22), the transformers are introduced by Reed

relay in the lead to output I. The 2dB divider stages in the 50 kHz section are also triggered by the output level switch. The four stages of 2 dB each are repeated after each 10 dB stage has been connected. With the output level switch it is possible to cover a level range of 0 to -78 dB in 2 dB stages.

Output II is taken off before the transformer chain. As a result the frequency response resulting from the divider transformers is eliminated at this output. The level at output II corresponds at $R_i = R_a = 75$ Ohm to the display reduced by 10 dB on the transmission level instrument at all full 10 dB positions of the output level switch and in the voltage level operating mode (0 dB $\hat{=}$ 0.775 V).

Transmitter blanking fulfils the following functions:

1. Switching off the instrument display
2. Time staggering of individual disconnection
3. Shut-off of the 24 MHz AGC amplifier and of the differential amplifier
4. Switching off the excitation of relays 601 - 605.
5) Switching off the 24 MHz oscillator.

The following is a summary of the time staggering:

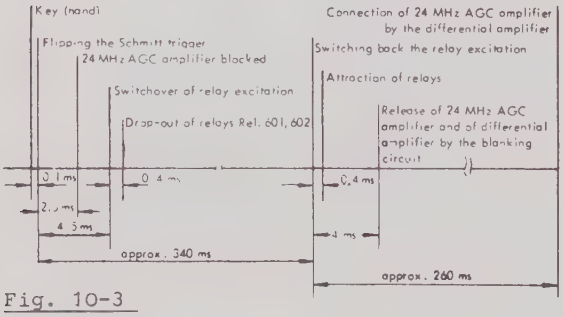

Key (nand)
Flipping the Schmitt trigger
24 MHz AGC amplifier blocked
Switchover of relay excitation
Drop-out of relays Rel. 601, 602
Connection of 24 MHz AGC amplifier by the differential amplifier
Switching back the relay excitation
Attraction of relays
Release of 24 MHz AGC amplifier and of differential amplifier by the blanking circuit
0.1 ms
0.4 ms
0.4 ms
2.0 ms
4.5 ms
approx. 340 ms
approx. 260 ms

Fig. 10-3

10.1.5. Modulation input

At the back of the set there is a modulation input.

The jack at the modulation input takes the form of a switch jack. When a plug is inserted the power supply for the 50 kHz section is interrupted, i.e. the level control and level display (I 701) are rendered inoperative.

The AGC amplifier now functions as a modulation stage. The operating point is such that the transmission level at the output of the output amplifier is 6 dB lower than the maximum level. This permits modulation of 100 % without overshoot of the amplifiers taking place.

The modulation sensitivity is approx. 2 mV for m = 1%. The modulation frequency is 0 to 100 kHz. The modulation distortion is approx. 5% at modulation of m = 50%. With greater modulation the distortion increases sharply as a result of non-linearity of the characteristic of the AGC amplifier. At high modulation voltages (max. 10 V_{eff}) it is also possible for square wave modulation to be generated.

As the 50 kHz section and the control loop are out of operation the transmission level at the output can only be varied in steps of 10 dB. The level stability over the frequency range is no longer available either. It is advisable therefore to monitor the modulated output voltage with an oscillograph.

10.1.6. Sweep operation with WZ-6

With the WZ-6 the transmission frequency can be swept in the entire range. In this case the control time constant of the PS-60 is accelerated as from 1 MHz centre frequency.

10.2. Power supply (25)

The powerpack supplies the voltages necessary for operation. The 50 Hz mains voltage passes through fuse, mains filter, voltage selector to the mains transformer Ü 2501 and after voltage conversion and rectification supplies 5 DC voltages. These are regulated or stabilized according to requirements in the subsequent IC standard regulators.

By means of standard regulators the voltages of +12 V, - 12 V and +5V are generated in IC's 2501, 2502 and 2503 with the corresponding power transistors T 2503, T 2505 and the Darlington stage T 2508 and T 2507.

The voltage of +200 V necessary for operation of the counter display (21) is only stabilized. For this purpose the Z-diode Gl 2502 is used in combination with the transistor T 2501 connected as emitter follower.

Also stabilized only is the supply voltage for the output amplifier (4) of -14.4 V. This voltage is composed of the -12V voltage and a -2.4 V voltage. The 2.4V voltage is obtained through three diodes Gl 2510 ... Gl 2512, through which passes the entire current of the -12V voltage.

10. DESCRIPTION OF FUNCTION

10.3. 1 MHz oscillator and pulse shaper (11)

The 1 MHz oscillator supplies the internal standard frequency of the PS-60. This is used for synchronization of the 24 MHz oscillator. In addition the frequency reduced by the factor 100 is used as time base for counter (21) for frequency display. In the case of external control the oscillator is switched off and the 1 MHz signal from the receiver fed into the pulse shaper through Ü 1101.

Function of the circuit:

The 1 MHz oscillator operates in capacitive three-point circuit. Its frequency determining elements are C 1102, C 1103, C 1105, C 1106 and Q 1101.

The crystal operates in the inductive range of its resistance characteristic.

The T 1101 of the oscillator transmits the oscillator AC voltage through C 1107 to the emitter of T 1102. Through the tapping of Ü 1101 the 1 MHz signal is transmitted to the base T 1103 in the case of external control.

Ü 1101, C 1109, C 1110 and 2.2 nF which are located at point 4 off board 610-H form a resonant circuit which is balanced to 1 MHz.

C 1111 is also at the collector of T 1102. The function of C 1111, R 1111 and the base emitter diode of the T 1102 is to be compared with that of a peak value rectifier. If as a result of the base emitter diode of the T 1103 the current i_B of the peak rectification is flowing, a far higher current will therefore flow through the emitter collector section of T 1103 $i_B.ß$.

As a result a voltage drop occurs across R 1112. The T 1105 opens and passes positive base voltage pulses to T 1104 through differentiator R 1115, C 1114. T 1104 opens and connects the base of T 1106 and T 1107 to chassis. T 1106 closes and T 1107 opens.

To ensure considerable slope (5 ns) of the starting flank of T 1107, T 1105 and T 1104 are coupled to one another through C 1113 and C 1114 respectively so that commencement of switch-on of T 1105 initiates the feedback process and causes it to take place independent of the further activation of T 1105.

The resultant pulses with steep starting edges are made available at points 1 and 3 of the phase comparison circuit.

10.4. Control oscillator (12)

Function in the set:

The control oscillator permits tuning of the PS-60 over the entire reception range in one range. In a phase control circuit it synchronizes the carrier oscillator (16) which directly determines the transmission frequency. Thus the stability of the control oscillator is solely responsible for the stability of the transmission frequency. (See also Description of Function of complete unit point 10.1.).

More detailed description of the oscillator circuit is unnecessary as the oscillator is produced under its own type number (BN 640) and is therefore described elsewhere.

Switch S 1 is mechanically coupled to the "coarse-fine" selection of the tuning knob and switches over the time base in the counter and thus the resolution of the digital display.

10.5. 3 : 1 divider (13)

The carrier frequency of 24 MHz to 42.6 MHz is divided 1 : 3 in the divider.

The circuit consists of two buffer stages (T 1303, T 1301) a limiter (T 1302, T 1303) and the IC divider (IC 1301).

The low resistance base voltage generation for the limiter and a buffer stage takes place with a collector stage (T 1304).

The modulation circuit for IC 1301 fulfils two important requirements:

1) Generation of a TTL-level for the IC divider
2) Decoupling of the IC input from the input of the complete circuit.

Re.1) The relatively high divider frequency requires rapid switching times of the limiter transistors. The parasitic capacitances must be recharged rapidly. For this purpose low resistance operating resistors(R 1307) and thus high currents are necessary. The limiter current is approx. 40 mA. To achieve short switching times in the limiter it is heavily overdriven.

The buffer stage T 1301 operates as base stage and has a resonant circuit as external resistance. This is designed so that together with the transistor and switching capacitances it is tuned to the effective frequ-

ency band centre (fm ≈33 MHz). Limitation is effected with diodes Gl 1301 and Gl 1302. The activation voltage for the limiter is $E_{st} \approx 1.2$ V_{pp}.

Re.2) Feedback of the IC's to the emitter of the T 1305 as well as mixer I causes interference lines with the modulation frequency 1/3 × $f_{Carrier}$.
In order to obtain maximum possible signal-to-noise ratio the two buffer stages T 1305 and T 1301 are necessary. The first base stage has a transformer in the collector which acts as current transformer and simultaneously as high-pass filter. The transformed current is so high that limitation takes place at the external circuit of the second base stage. The actual divider is formed by two correspondingly connected JK - FF's.

10.6. Phase comparator (14)

The 8 to 14.2 MHz square wave oscillation with a pulse duty factor of 1 : 2 supplied by the 3 : 1 divider (13) is compared in a ring modulator with the reference frequency of the control oscillator (12).

The diodes Gl 1401, Gl 1403 and Gl 1402, GL 1404 are alternately switched by the limiter stage T 1401, T 1402 in time with the control oscillator (12). The pulse duty factor of this oscillation is automatically kept at 1 : 1 by the electrical separation of the two emitters and RF coupling with C 1404 (pulse duty factor regulation).

By means of the bridge of the diode pairs connected and of the transformer Ü 1401 points (1) or (4) of transformer Ü 1402 are alternately connected to chassis,

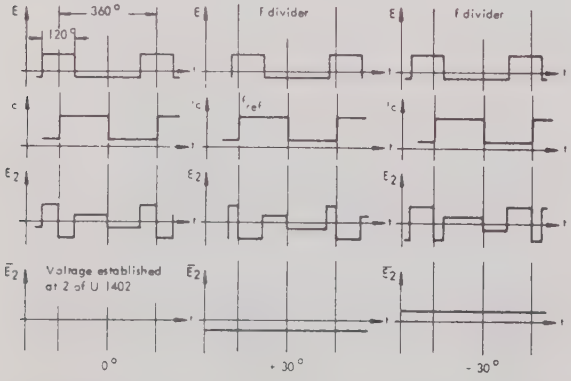


Fig. 10-4

Illustration of phase displacement (f_{ref} -f Divider) with loop locked on.

i.e. Quasi polarity reversal of the voltage (3 : 1 divider) at points (2), (3) of Ü 1402.

Through R 1410 coupling out takes place of the resultant mixture products (that is to say sum and difference frequency). The sum frequency (with control circuit locked on) is equal to double the reference frequency, the difference frequency has a frequency of zero, that is to say a DC voltage E_2. Its magnitude and polarity depend on the phase difference of the two frequencies.

The voltage E_2 readjusts the carrier oscillator (16) through the equalizer (15).

A low-pass filter (C 1407, L 1401, C 1406 and C 1408) with the cut-off frequency of 3 MHz clips the AC voltage components occurring during mixing. With the further low-pass filter C 1409, R 1412 and C 1410 the loop gain is reduced as from 200 kHz to 0 dB thus ensuring the stability of the control circuit.

10.7. Equalizer and search oscillator (15)

The phase comparator (14) supplies a voltage of approx. ± 0.2 V which is obtained in linear fashion from the phase shift of ± 60°. In linear fashion with this phase shift the frequency of 42.6 to 24 MHz of the carrier oscillator (16) should be fully advanced. The voltage range necessary for this purpose is approx. ± 11 V.

The module (15) consists essentially of a degenerative differential amplifier. Equalization of the oscillator characteristic takes place in the negative feedback branch with components R 1514, R 1515 and Gl 1503 at the inverting input to T 1501.

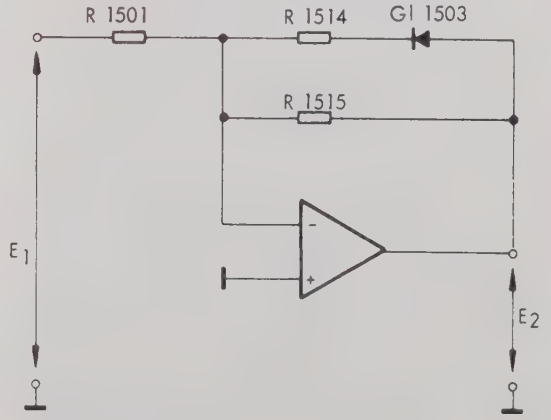


Fig. 10-5

10. DESCRIPTION OF FUNCTION

With positive control voltage E_1, i.e. negative voltage E_2 at the amplifier output diode Gl 1503 is blocked. Then only R 1515 is included in amplification. If E_2 is driven to positive values and if the switching threshold of Gl 1503, approx. 0.5 V, is exceeded, gain will be determined by the parallel circuit R 1515 with T 1514.

At the same time the differential amplifier is connected as oscillator which can only oscillate when the control loop has not locked on or vice-versa, the search oscillation breaks down momentarily on reaching state of engagement.

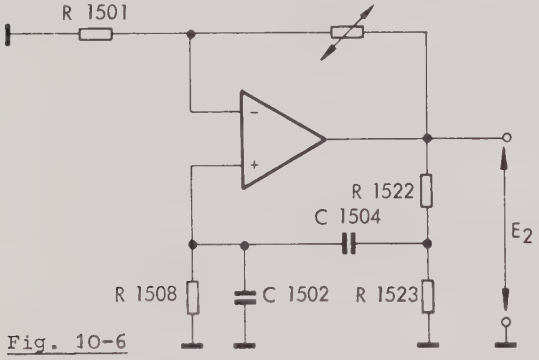


Fig. 10-6

The components R 1508, C 1502, R 1522, R 1523 and C 1504 represent a Wien bridge through which positive feedback takes place to the non-inverting input T 1502. The positive feedback is kept within limits by the voltage divider R 1522 and R 1523 such that oscillation occurs (f ≈ 4 Hz) which is approximately trapezoidal.

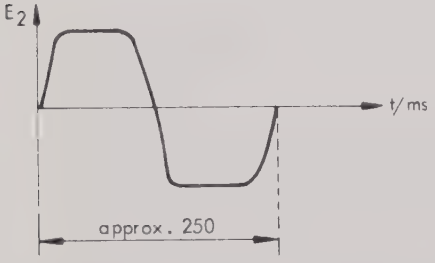


Fig. 10-7

The amplifier itself consists of a differential input stage (T 1501 and T 1502), the amplifier stage with T 1503 and the output stage consisting of T 1505 in combination with T 1504 and the constant power source T 1506. The exact position of the operating point of T 1501 and T 1502 is adjusted with the voltage divider R 1506, R 1512, R 1510, R 1509 as well as P 1501. The diodes Gl 1501, Gl 1502 replace the emitter resistance for operating point adjustment. The voltage drop is largely independent of the emitter current flowing with at the same time low differential resistance. Thus the negative feedback is also low for the DC currents. C 1503 assumes this function for higher frequencies.

The elements R 1507 and C 1501 guarantee natural stability of the stage. The output resistance of the equalizer amplifier should be kept as low as possible. This is effected by the emitter follower T 1505 in combination with the constant power source T 1506. By extension with T 1504 it is also possible to achieve rapid recharging of a capacitive load to negative potential. The subsequent carrier oscillator forms a capacity load. R 1525 prevents possible tendency to oscillation which can be caused by this load.

10.8. Carrier oscillator (16)

The carrier oscillator supplies the carrier of 24 to 42.6 MHz for the transmission mixer.

The oscillator consists of a pronounced positive feedback differential amplifier (T 1601, T 1602).

A resonant circuit tunable with capacitant diodes is its external resistance.

Part of the resonant circuit amplitude is tapped off at coil L 1602 and applied to the base of T 1602 (inductive three point oscillator).

This high resistance positive feedback is such that the differential amplifier is considerably overdriven. (This has a favourable effect on the noise behaviour of the oscillator. The diode Gl 1604 limits the amplitude of the oscillator to $E_{OSC} \approx 0.6\ V_p$.

The cathodes of the capacitance diodes are applied to the + 12 V potential. As a result a maximum control range of approx. 23 V is achieved because the activating voltage can be a maximum of $E_{st\ max} \approx -11$ V.

The resonant circuit is designed so that high operating quality is obtained with a wide tuning range. For this purpose three capacitance diodes are necessary. The outputs are isolated from the actual capacitor by a Darlington circuit for decoupling. The input resistance of the buffer stage is very high as a result of a bootstrap circuit (C1609, R 1611). For this reason the resonant circuit is only slightly loaded.

10. DESCRIPTION OF FUNCTION

The supply voltage of the buffer stage is filtered separately in order to prevent the reaction of the 3 : 1 divider stage on the capacitant diodes.

In the case of external control the carrier signal does not pass from the oscillator but from the external control input through Gl 1606 to the buffer stage. The operating voltage of the oscillator is then switched off.

10.9. Frequency divider (20)

The frequency divider fulfils two functions:

1. Level matching to C - MOS - IC.
2. Frequency division of 100 : 1 for the time base of the frequency counter (21).

Level matching is effected by means of a buffer stage with bootstrap input which is followed by a switching stage (T 2003).

As external resistance of T 2002 a resonant circuit has been used to obtain high AC voltage output resistance.

IC 2001 divides the 1 MHz signal to 10 kHz. The output signal has a pulse duty factor of 5 :1.

10.10. Counter and indication (21)

10.10.1. Counter module BN 611-N

The "Counter module" consists essentially of an asynchronous counting circuit and an intermediate storage as well as a decoder driver for each decimal place.

The control pulses are supplied to the counter from the "Time base module" (BN 611-R): "Buffer" pulse through point 49, "Reset" pulse through point 50.

A counter cycle is divided into three main sections:
(See pulse diagram Fig. 10-8).

1. Counting in
2. Buffering
3. Resetting the counter.

Through two inputs, points 45 and 46 counting in can take place. In the operating mode "Gate time 12 ms" the AND-OR gate IC 2120/2.1 receives the H-signal at PIN 3 through point 47 of the time base. As a result the first BCD counter (IC 2118) is switched off by the following counter section and simultaneously by IC 2116 the last decimal place (100 Hz digit) through the BLANK input. The counted-in pulses pass through point 46. In the operating mode "Gate time 120 ms" the first counting stage is recoupled (point 47 = L) through the AND-OR gate IC 2120/2.1. Point 48 receives from the time base H-signal with which then counting in is carried out through point 46 and PIN 1 of the AND-OR gate IC 2120/2.2. In the operating mode "Gate time 300 ms" the pulses pass through point 45 (point 48 = L). In this case the digital error suppression circuit mounted on card BN 611-R is inoperative (is bypassed in the signal flow). Because at 300 ms gate time the total counter contents appear shifted to the left by 1 digit, the leading zero suppression is switched off at IC 2101 through point 48.

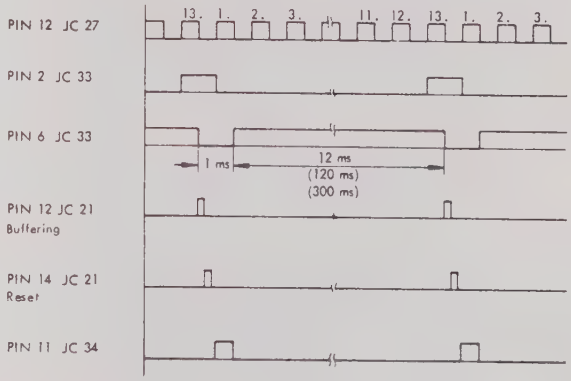


Fig. 10-8

10.10.2. Time base BN 611-R

On board BN 611-R are mounted the time base with the counter control and a circuit for suppression of the digital error.

Essentially the time base consists of a switchable frequency divider which acts on a gate FF. The "Gate open signal" generated by the gate FF can last 12 ms, 120 ms or 300 ms. The corresponding cycle times are 13 ms, 121 ms or 301 ms.

The 10 kHz signal fed in through Bu/St 2102 is first of all frequency divided in the ratio of 10:1 by the counter CD 4017 AE (IC 2127). At the counter output 1 ms pulses are therefore available which are passed to the subsequent 9-stage binary divider (IC 2128 and IC 2129). The gate FF IC 2133/2.1 is connected to the binary divider through a selectable decoder for the binary state 12, 120 and 300.

If, for example, the gate IC 2131/3.1 is selected for the state 12 (12 ≙ LLOO),

the D-input of the gate FF is primed (see pulse diagram) with the front edge of every 13th pulse. With the rear edge of this pulse the FF is set and after 1 ms reset again with the rear edge of the first pulse of the new measurement cycle. A signal is obtained therefore for control of the counter gate IC 2123/3.3 which opens the gate for 12 ms and blocks the gate for 1 ms. During the 1 ms interval the binary counter is reset and through the gate IC 2126/2.1 + 2 the control pulses "Buffer" and "Reset" are generated. For this purpose the decoded outputs 6 and 8 of the 1st 10:1 divider IC 2127 have been used at which 100 µs pulses can be taken off.

By switching over the decoding it is possible to select the gate times of 120 ms and 300 ms. This takes place through the 2 switches S 201 and S 1. S 1 is located in the control oscillator and is connected via Bu 1/3.

At the fastest sampling rate, i.e. gate time 12 ms, both switches emit L-signals (low) to gates IC 2134/3.2 and IC 2135/4.1. Through IC 2134/3.2 gates IC 2135/4.2 is primed for the reset signal coming from IC 2126/2.2 whereby the FF IC 2133/2.2 is moved to the position in which the decoder switches state 12 to the gate FF. By actuating one of the switches S 1 or S 2101 gate IC 2134/4.2 is blocked and gate IC 2135/4.4 is primed. When the measurement cycle has elapsed FF IC 2133/2.2 is now reversed with the reset signal and the decoder switches to the 120 ms gate time.

By linking the switchover to the reset signal it is thus possible for the time base to be switched over from 12 ms to 120 ms measuring time (or from 120 ms to 12 ms) only within the 1 ms measuring interval.

If both switches S 1 and S 2101 are operated gate IC 2131/3.2 and thus the 120 ms cycle are switched off through IC 2135/4.1. By switching off the 121 ms cycle the binary divider automatically counts up to the next decoded state (300). Switchover of the measuring time from 120 ms to 300 ms takes place therefore without buffering as a result of which the measuring cycle running at the time is "gated".

As already mentioned above the BN 611-R contains a circuit for suppressing the digital error of the frequency display.

The essential component of this circuit is an offsettable 4:1 divider.

This 4:1 divider emits a transfer pulse to the subsequent "Actual" frequency meter after each divider cycle. In order not to falsify the display of the frequency meter the 4:1 pre-division is corrected by extending the measurement time by the factor 4.

Seen as a whole therefore an additional divider stage is connected in series with the "Actual" frequency meter.
If one examines the composition of these two frequency meters (4:1 divider and frequency meter) as regards the digital error 2 basic features of behaviour can be distinguished:

1. The digital error acts in the prescaler in a way such that from measurement to measurement the divider cycle will just run completely through on the one hand and then again will not. This has the consequence that the transfer pulse occurs in the same rythmn. In the end effect however the displayed result of the subsequent frequency meter also changes in this case from measurement to measurement.

2. The digital error has the effect in the prescaler that the character set available is used without the total number of transfer pulses emitted changing from measurement to measurement. Thus in this case the displayed result is steady in the subsequent frequency meter.

The above is valid for a prescaler which is preset at the beginning of each measurement cycle to any selectable but constant initial state (e.g. zero).

The basic conception which is embodied in the digital error suppression circuit is in fact to ensure by rational presetting of the prescaler to optionally 2 different initial values that the digital error can always move within the number set of the prescaler without alteration of the number of transfer pulses.

The 4:1 prescaler(IC 2124) can be preset to 0 or 2. Connected to it is a decoder for divider states 0 and 3 (LL and HH, IC 2123/3.1 and 3.2) and a memory which retains whether 0 or 3 was last decoded (IC 2122/4.2 and 4.4). Dependent on the position of the memory the prescaler will be preset at the cycle beginning to 2 (latterly 0 decoded) or to 0 (latterly 3 decoded).

The decoding is carried out in the measurement interval with the intermediate storage pulse. In the same way presetting of the divider takes place in the measurement interval with the reset pulse.

10. DESCRIPTION OF FUNCTION

If one assumes that first of all the prescaler is preset to 0 one obtains the following representation of the measurement sequence within the prescaler and the subsequent frequency meter:

Measurement No.	Prescaler cycle	Frequency display
1	01230123012	2(=Carry over)
2	012301230123 Frequency	
3	0123012301230increase	3

As now at the end of the cycle a 0 was decoded, presetting takes place to 2 before the next measurement:

4	2301230123012	3
5	230123012301...3	3

If as from and including the 3rd measurement the frequency remains constant the number of transfer pulses cannot change even with digital error as a result of changeover of the preset state as was indicated in the case of measurement No.5.

10.11. 24 MHz oscillator (18)

The 24 MHz oscillator supplies the signal which is converted in the transmission mixer with the carrier frequency to the transmission frequency.

The "24 MHz oscillator" module can be sub-divided functionally into three sub-assemblies:

1. 24 MHz oscillator (T 1807)
2. Search oscillator (T 1802, T 1805)
3. Phase comparison circuit (G1 1801 to G1 1804).

These three sub-assemblies are combined to form a closed control loop. The reason for this considerable circuitry is to be found in the frequency instability of the 24 MHz oscillator (LC oscillator). For this reason the 24 MHz is synchronized with the 1 MHz of the crystal oscillator and is then exactly the same as the 1 MHz.

10.11.1. 24 MHz oscillator

This oscillator operates in LC circuit. The phase rotation through 180° between base and emitter of T 1807 is achieved on the principle of the capacitive three-point circuit. Diode G1 1806 limits the oscillator AC voltage to 0.7 V single peak value, independent of the quality of the resonant circuit. The capacitance diode G1 1805 is connected DC voltagewise with its annode through L 1803 to chassis and can be influenced capacitively on the cathode by application of a positive voltage which leads to a corresponding frequency variation of the 24 MHz oscillator.

Through C 1815 the 24 MHz passes to the collector stage T 1806 and is decoupled at its emitter and made available to the transmission mixer through base stage T 1808 at point 10.

The base stages T 1804 and T 1801 are used for decoupling and amplification of the 24 MHz signal.

L 1804 and C 1807 are used to eliminate a 2 MHz interference in the SPM-60 and are not necessary for the transmitter.

In order to obtain a DC voltage-free signal point a L 1801 and L 1802 have been incorporated as load for T 1801.

10.11.2. Search oscillator

The search oscillator is an unstable DC voltage amplifier. If C 1808, C 1812 and R 1818 were not present it would be in the case of T 1803 and T 1805 a conventional differential amplifier with a DC current gain of ∿10. The operation of the search oscillator is practically the same when the 24 MHz oscillator is locked on. The search oscillator emits as a function of the voltage at C 1806 a proportionate voltage at the collector of T 1805. The range in which the voltage can be varied, i.e. the locking range of the 24 MHz oscillator is dependent essentially on the specification of R 1813 and R 1817. If the 24 MHz oscillator is not synchronized an AC voltage is present at point (13) whose amplitude however is not sufficient to fully drive the differential amplifier. This results in a narrower capture than locking range.

For correction of this error the differential amplifier has been equipped with positive feedback (C 1808, C 1812). The differential amplifier oscillates and displaces the voltage at the collector of T 1805 over the same range as is possible in the blocking range. (f of the search oscillator ∿ 20 Hz).

When the 24 MHz oscillator oscillates within the capture range extended by the search oscillator, its frequency is shifted through G1 1805 until it is synchronous with the 1 MHz. Thus the control circuit of 24 MHz oscillator/ phase comparator - search oscillator

is complete and compensates the internal feedback of the search oscillator by its variable gain, i.e. the search oscillator no longer oscillates.

The locking and capture range of the phase meter is conditioned by ageing, temperature drift and the instability of the 24 MHz oscillator. It is approximately 200 kHz.

If the search oscillator is constantly in operation, point a is connected to point b. Connection of point c to point d renders the search oscillator inoperative.

10.11.3. Phase comparator

The 1 MHz signal supplied at point 5 is converted by the blocking oscillator T 1802, Ü 1801 into pulses with defined properties. If a negative voltage reaches the emitter of T 1802 a current starts to flow through the transistor and Ü 1801, points 3-4. The feedback winding points 5-6 of the Ü 1801 amplifies the negative signal at T 1802 and as a result forces rapid closing of the T 1802 independent of the shape of the drive signal.

The same occurs when closing the T 1802. If the current through Ü 1801 cannot increase (R 1807 and 1804 limited to ~10 mA), the voltages at Ü 1801 change their polarity and block T 1802.

The pulses of the blocking oscillator open the diodes G1 1801 to G1 1804 for a few ns. During this time C 1806 either charges or discharges in the direction of instantaneous AC voltage amplitude at point a. (See Fig. 10-9). C 1806 thus integrates the momentary voltages at point a. The diodes are blocked during the pulse gaps by C 1804. A DC voltage at C 1806 indicates a fixed phase relationship between the two signals. An AC voltage at C 1806 indicates that the phases of the signals are passing through in oppostion to one another.

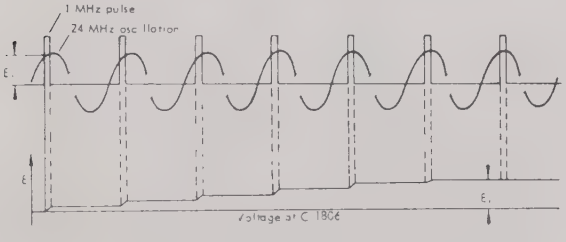


Fig. 10-9

10.12. 24 MHz control amplifier (10)

From the 24 MHz oscillator the 24 MHz character signal is passed through point (10) 4 of the base stage T 1003. The base stage supplies the 24 MHz current to the emitters of the differential amplifier T 1001, T 1002. The RF current which passes to T 1001 is diverted to chassis. (Through C 1005). The part which reaches T 1002 is passed on as useful signal. It reaches the output point (10) 3 through the 24 MHz band pass filter (L 1002, C 1006), the coupling capacitor C 1009 and the output stage T 1006.

Trimmer C 1008 is used for resonance adjustment of the 24 MHz circuit. With P 1003 the 24 MHz output level is adjusted. At the same time the tolerances of the entire control circuit are compensated. With modulation operation the modulation sensitivity is not affected by P 1003.

P 1004 is used for adjustment of the 6 dB jump (level reduction by 6 dB) in the case of modulation operation. At the same time however the output level is affected which is in fact undesirable. This output level effect is therefore compensated again with P 1003. Through transistor T 1004 the base voltage for T 1003 and T 1006 is generated with low resistance.

In the closed control circuit (complete set) the control voltage of the AGC amplifier is approximately "0 V" at maximum output level. This corresponds to an output voltage at point 3 of -16 dB. The required control range of the AGC amplifier is 44 dB. The actual control range of the AGC amplifier is however 53 to 60 dB so that there is sufficient reserve.

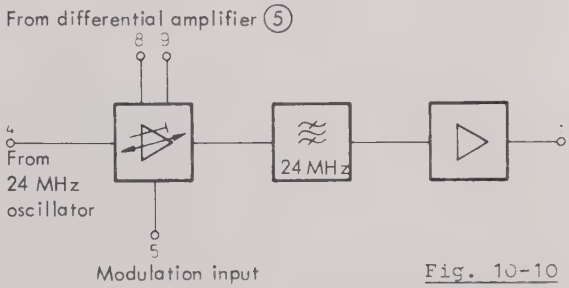


Fig. 10-10

Modulation circuit

The modulation capacity of the PS-60 is realized in the 24 MHz AGC amplifier. Through jack 1001 the modulation voltage is passed to the differential amplifier stage T 1001/T 1002. After supplying

the modulation frequency to the input jack, the power supply of module (7) (50 kHz section) is interrupted by the switch contacts. This has the result that the AGC amplifier is completely blocked through the differential amplifier (5). As in this state sine wave modulation is not possible, the modulation operating point must first be adjusted, i.e. the blocking voltage present at the differentail amplifier T 1001/ T 1002 must be compensated. For this purpose the compensation voltages of -12V and +12 V are passed through switch jack 1001 to points (10) 6 and (10) 7. With P 1001 and P 1002 accurate compensation adjustment is carried out. The operating point of the differential amplifier is approximately "0 V" after adjustment.

So that with m = 100% the subsequent amplifiers are not overdriven (pre- and output amplifier), during modulation operation the output level is additionally attenuated by 6 dB. For this purpose the transistor T 1005 is used which is switched on through switch jack 1001.

The 6 dB level reduction is achieved by the collector resistance R 1017 (820 Ohm) being parallel in switched state to the output resistance of T 1002 which is also 820 Ohms.

Data on the modulation circuit:

Modulation voltage: 0 to 10 V_{eff}

Modulation frequency: 0 to 100 kHz

Modulation sensitivity:
approx. 2 mV/% modulation.

10.13. 24 MHz low-pass filter ⑨

The 24 MHz low-pass filter has a cut-off frequency of 28 MHz (L 901 ... L 904).

The low-pass filter requires power supply at the input and at the output a terminating resistance of 75 Ohm. The power supply is effected through transistor stage T 1006 in the 24 MHz AGC amplifier.

The DC current path for the collector of T 1006 in the 24 MHz AGC amplifier leads through the 24 MHz low-pass filter (9) and the 75 Ohm resistance in the transmission mixer (1) to chassis. The 75 Ohm resistance in the transmission mixer simultaneously forms the terminating resistance for the 24 MHz low-pass filter.

The main function of the 24 MHz low-pass filter is to transfer the signal frequency (24 MHz)from the AGC amplifier and to suppress the harmonics of 24 MHz. Harmonics would generate undesirable mixture products in the transmission mixer.

The following approximate harmonic ratios are achieved:

$$aK_2 = 90 \text{ dB}$$
$$aK_3 = 100 \text{ dB}$$

10.14. Prelimiter and generator mixer ①

The limiters produce an approximately square wave voltage from the sinusoidal carrier voltage. The end limiters (T 104 and T 105) and the 2 prelimiters have been connected in series DC currentwise in order to save current.

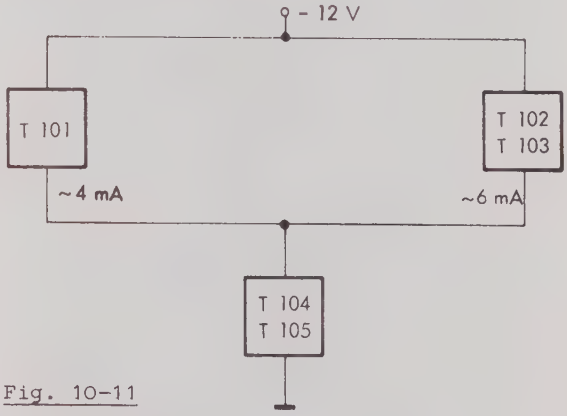


Fig. 10-11

The high-pass filter (C 101 and L 101) at the first limiter stage is intended to suppress 1 MHz residues. The second stage is electrically coupled to the first, the third to the second through an 82 pF coupling capacitor. The control voltages between the limiters are kept to a minimum in order to keep overshoot on the top of the carrier square wave within limits as far as possible. Thus the control voltage at the input should if possible not exceed 0.75 V. The 27 µH chokes in the emitter leads are used to steepen the square wave edges and in the collectors of the second prelimiter to save voltage. At the end limiter if possible a square wave voltage without overshoot should ideally be present, but this is hardly achieveable in practice.

The two transistors T 106 and T 107 on the mixer board supply the low resistance base DC voltage for the limiters. Through the opposed connection of the base emitter sections of T 106 and T 107 with the appropriate limiter transistors the

temperature dependent threshold drift is compensated.

In the case of the transmission mixer this is a ring modulator.

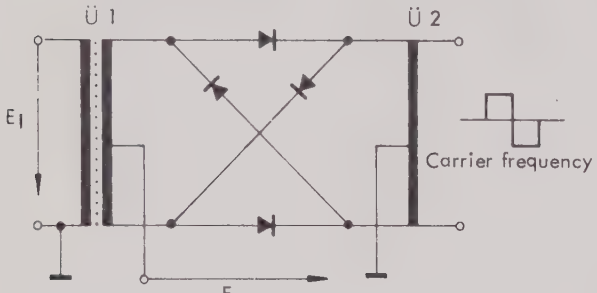


Fig. 10-12

In the case of the practical version used here the carrier and output voltages have been changed over in contrast to the basic circuit diagram. The carrier voltage (through T104 and Z 105) in each case connects an external point of the transformer 2 to chassis so that the polarity is reversed.

The mixer input is fed from approximately 5 Ohm and for the mixture product terminated with 250 Ohm. From the attenuation of the voltage divider at the input and the mixer attenuation a total conversion attenuation results as follows:

$$a_R = 20 \lg \frac{75}{5.6} = 22.3 \text{ dB}$$

$$a_M = 20 \lg \frac{2}{\tau} = \frac{3.9 \text{ dB}}{26.2 \text{ dB}}$$

The input resistance results, as the low-pass filter (20 MHz-TP) for the character is high resistance, essentially from the series connection of the resistances of the voltage divider at the input:

69.4 Ohm + 5.6 Ohm = 75 Ohm

With ideally symmetrical ring modulator the following mixture products appear at the mixer output:

Ω + W, Ω - W, $\Omega \pm$ 3 W, 3$\Omega \pm$ W

(Ω = Carrier frequency, 24 to 41 MHz, W = Signal frequency 24 MHz).

The mixture product Ω - W is used in our case as useful signal. Apart from the products $\Omega \pm$ 3 W and 3$\Omega \pm$ w, which are not in the useful range in practical trial the mixture product 2 W-Ω, also appeared which is in the useful range and should therefore be specially noted.

10.15. 20 MHz low-pass filter (2)

The 20 MHz low-pass filter is a Cauer filter of the 10th order where both in the pass and in the cut-off band a constant attenuation value is approximated in the Tschebyscheff sense. The filter has been designed for a reflection factor of 31% in the pass band at the input, related to the terminating resistance R_a = 250 Ohm.

In the complete set it represents the connecting element between mixer and preamplifier. It is used for filtering out the carrier fundemental wave and the upper side bands. The stop band attenuation in the range of the carrier fundemental wave (24 - 42.6 MHz) should be $a_{sp} \triangleq$ 100 dB, the ripple in the pass band for $\leq$ 17.1 MHz should be a $\leq$ 1 dB.

As it is a Type 0/1 filter, i.e. R_V=0 and 0< R_a < ∞, tolerance fluctuations of the shunt capacitors, inaccurate adjustment of the peak circuits and errors in the terminating resistance have a more unfavourable effect on the forward wave than is the case with other filters. It is therefore necessary to provide facility for correction of such fluctuations by means of the coil L 201 and the trimmer C 209.

10.16. Preamplifier (3)

The preamplifier is used for amplification of the mixer signal by 37 dB. Its input at the same time represents the termination of the 20 MHz low-pass filter. The design of the preamplifier is determined by the low maximum current (11.8 mA) and the required absence of distortion (a_K < - 50 dB).

The signal passes through the coupling capacitor(C 301) to the input of the differential amplifier (T 301/T 302), whose operating point can be adjusted with potentiometer(P 301). From the collector of T 302 the signal passes to the input of the second differential amplifier(T 303/T 304), whose operating point is adjusted with P 302. With this operating point shift it is possible to cause the differential stage to distort. As however this distortion is compensated by the distortion of transistor T 305, P 302 can be adjusted to the K_2-minimum on a frequency. This is best done at a point at which the distortion is unfavourable (for example at 10 MHz).

From the transistor T 305 the signal is fed back frequency independent to the base of transistor T 304. The bootstrap

circuit at the second differential amplifier improves the distortion as the emitter resistance is increased dynamically and as a result a lower distortion current can flow through R_E.

From the emitter of transistor T 305 the amplified signal passes to a low-pass filter. This low-pass filter causes both improvement of distortion in the pass band and additional attenuation at high frequencies for improving the stop band attenuation of the 20 MHz low-pass filter. The second capacitor of the filter takes the form of the input capacitor of the output amplifier.

As this input capacitance is dependent on the construction and transistor specification, the forward ripple of the filter will fluctuate slightly which can however to a large extent be corrected by coil L 201 of the 20 MHz low-pass filter.

10.17. Output amplifier ④

The output amplifier can be divided into 4 individual stages:

AGC amplifier	T 401 ... T 403
Preliminary stage	T 404 ... T 406
Driver stage	T 407 ... T 408
Output stage	T 409 ... T 410

By comparison with the voltage divider R 403/R 404 the AGC amplifier fixes the operating point of the driver stage and thus voltagewise of the output stage as well.

The filter capacitance C 404 is increased by the factor 20 by T 403, R 411. In comparison with a correspondingly high capacitance against chassis this circuit has the advantage of faster settling of the control loop after overshoot.

Overshoot occurs primarily when the unit is switched on. As long as stage T 403 is overdriven C 404 is not increased.

The preliminary stage consisting of the differential stage(T 404/T 405) and the subsequent emitter follower(T 406) supplies the necessary voltage amplification. Without negative feedback (base T 405 blocked) the gain at low frequencies (according to the position of P 401) is 33 to 38 dB, with negative feedback (through the divider R 417/R 418) it is 13.4 to 13.8 dB. The input resistance of the amplifier at point 4 is approx. 20 kOhm ∥ 6 pF. This input resistance represents the termination of the low-pass filter in the preamplifier.

With P 401 it is possible to adjust the current distribution of the differential stage and thus the K_2-symmetry of the preliminary stage without altering the DC voltage values. This adjustment is effective primarily at high frequencies. The K_2 adjustment at low frequencies is obtained with P 403. Thus the centre DC potential of the output stage is displaced across the operating point-AGC amplifier (T 401 ... T 403).

Choke L 402 provides boosting of the negative feedback factor and thus phase lag of the ring amplification above the useful frequency range. The negative feedback of the preliminary stage produces increase of the input resistance and lowering of the output resistance. As the ring amplification however, starts to drop at approx. 10 MHz, the output resistance receives a considerable inductive component so that the stability of the subsequent driver stage must be ensured by unusually high base series resistances.

The driver and output stages formed from collector stages provide current amplification and adequate freedom from reaction so that changes in the load resistance of the complete amplifier do not affect the negative feedback loop of the preliminary stage to any extent. The chokes L 404 and L 405 raise the load resistance of the driver stage at high frequencies and thus reduce their modulation.

The emitter current of the output transistors is stabilized by the voltage drop at the common emitter resistor R 438 + P 402 + R 441 + R 439 and is adjusted by means of P 402 to the nominal value of 35 mA. Driver and output stages are constructed in themselves and complimentary to one another whereby excellent K_2-symmetry and temperature compensation are achieved.

The loading at output point 2 is dependent on the level setting selected in the output section, on the transmission frequency and the load resistance connected to the transmitter output.

The loading (impedance) is 28 to 300 Ohm:

The overall gain of the output amplifier is approximately 13.5 dB.
Maximum output level +7dB.

10.18. 50 kHz section ⑦

The 50 kHz board supplies the reference voltage for the differential amplifier variable by approx. 32 dB. The same

voltage is displayed on the instrument instead of the output level. This solution provides the advantage of being able to use a linear average response rectifier in the display circuit. Its frequency dependence is not disturbing here (thus the relatively low fixed 50 kHz frequency).

In contrast, the peak rectifiers at the differential amplifier input have a low frequency response and their unfavourable linearity deteriorates on account of the differential operation. As oscillator the circuit described in technical test report No. 142 is used.

This oscillator has an output voltage proportionate to its operating voltage, its amplitude stability being ensured by the stabilization of the operating voltage. This operating voltage is generated by means of G1 704 and IC 701. It is largely independent of the supply voltage (± 12V). At the same time G1 704 acts as reference for the supply current generator. The oscillator circuit consists of a resonant circuit of high quality in the collector circuit of a transistor. The control signal consists of short starting pulses which coincide at a maximum with the resonant circuit voltage. Thus the resonant circuit is charged up to the amplitude of its operating voltage at the beginning of each cycle and in the remaining section of the cylce the circuit oscillates freely. The short starting times are achieved by means of high feedback voltage, the pre-displacement of the starting phase by suitable under-dimensioning of the feedback capacitor C 704. With an additional series resistor T 705 as well as a relatively high capacitance C 703 in the base circuit the stop condition can also be fulfilled.

The AGC amplifier consists of a differential amplifier and a subsequent complimentary impedance transformer stage. The differential amplifier receives its control from a temperature compensated (G1 701) emitter stage which is fitted as common emitter resistance. In this stage (T 702, T 703) continuous level adjustment is carried out. With the aid of the base voltage adjustment at T 703 the voltage distribution (and thus the control signal) can be adjusted within the 20 dB range. One of the two transistors has as collector resistor a band pass filter (C 712, L 701) which contributes to improving the distortion ratio at the output. A buffer stage with T 705 and T 706 follows. After the TP 701 the output level branches on the one side to the 20 dB divider and on the other side to the display circuit.

The display circuit consists of a demodulator and a supply current generator. The demodulator - (in fact a rectifier stage) - has selectable emitter resistances. By this means the current of the rectifier diodes is adjusted according to the circuit type selected ("2 dB" or "20 dB").

In the "2 dB" range the previous last quarter scale graduation is spread over the entire scale width (from -2.2 dB to + 0.3 dB). This is achieved on the one hand by the current belonging to 0 dB being multiplied and on the other hand three-quarters of this current being diverted through a parallel connected current generator. Thus only the last quarter of the current will generate pointer deflection. Because however its range corresponds to the full instrument current this part is extended over the entire scale.

The supply current generator is related to a temperature independent reference element (T_K : 2 . $10^{-5}/^{o}C$). It is connected to the positive input of the differential amplifier IC 702 whose negative input receives the control voltage from the actual supply circuit.

The output signal of this differential amplifier is therefore exactly readjusted to the required current of the transmission transistor (T 709). As the reference element G1 704 and the supply current resistance(R 733, P 707) relate to the same voltage (-11.4V) the influence of the supply voltage is negligeable.

The 2 dB divider (combined with 10 dB output divider) permits varying the output level over its entire range in 2 dB stages. It consists of a divider transformer (Ü703), whose tappings are selected by switching transistors (BSY 80).

After the switching transistors for the 2 dB steps there follows a buffer stage with two complimentary transistors (T 725, T 726). This is designed so that it can supply the peak current for the following rectifier so that minimum possible distortion occurs because this falsifies the 2 dB divisions.

To keep divider error to a minimum in the 0 to - 78 dB settings a correction circuit must be used which prevents the divider error increasing for decreasing output level, because on account of connection of divider transformers increase of the residual attenuation takes place in the output section.

The correction stages used therefore in the 50 kHz section which as required produce 3 to 4 mB additional attenuation keep the divider error within narrow limits over the entire range (0 to - 78 dB). The following corrections are obtained:

- 2 mB from - 20 dB to - 28 dB
  and - 60 dB to - 68 dB.

In the set correction takes place by connection of 12 kOhm (division with R 724) with T 722, T 723 and T 724. In this case T 724 is operated with its base emitter section in the breakdown area and thus fulfils the function of a Zener-diode.

10.19. Differential amplifier ⑤

The differential amplifier is a two-stage DC amplifier with switchable "1-frequency". In it a control voltage is obtained by comparison of the 50 kHz reference voltage with the transmission level, this controlling the AGC amplifier (10). Its total gain is 74 dB.

The first amplifier stage consists of a differential stage with impressed emitter current and a gain of 40 dB. With potentiometer P 501 it is possible to correct the difference of the base emitter voltages of T 501 and T 501' as well as the forward voltages of the two peak rectifiers Gl 601 and Gl 602 (in the output section) (zero correction). The two diodes Gl 503 and Gl 504 protect the input transistors from saturation (e.g. during transmitter blanking). Through diodes Gl 501 and Gl 502 it is possible to achieve positive blocking of the input transistor in the case of defect indication and transmitter blanking.

The low-pass filter R 540/C 514 at the base of T 501 smooths the saw tooth residual ripple of the 50 kHz peak rectifier (Gl 601).

The second amplifier stage consists of a highly degenerative operation amplifier(IC 501). As a result of the symmetrical layout of the negative feedback elements at both inputs the gain Vo is as follows:

$$V_o = \frac{R520}{R510} + \frac{R518}{R504} = 2 \cdot \frac{1MOhm}{39\ K} = 34\ dB$$

The RC networks in the negative feedback branch and the staircase elements R 523/C 510 as well as R 537/C 511 and R 538/C 512 ensure the required gain reduction above the frequency and the required safety of the entire control circuit against oscillation.

With T 504 it is possible to switch off capacitor C 506 whereby the control circuit is accelerated as a result of displacement of the "1-frequency". Thus on sweep operation the frequency response of the modules (1) to (4) can be regulated. For acceleration of the peak rectifiers it is possible in this state to increase the standard supply current(R 502 and R 511) by parallel connection of R 501 and R 512 to T 503 from 12 µA to approx. 35 µA. With buffer stage T 505 the control voltage is coupled to the AGC amplifier. R 530 limits the range of modulation in positive direction and Gl 507 in negative direction.

In the case of positively or negatively overdriven operation amplifier the Schmitt trigger is connected through point 6 into the blanking for switching off the indicator (see also blanking circuit (24)).

10.20. Output circuit ⑥

From the output amplifier (4) the signal passes through Bu 601 to the output circuit. At the input of the first divider transformer (20 dB) application of the peak rectifier Gl 601 takes place to which the control loop (see block circuit diagram, complete unit) monitors or stabilizes the AC voltage level at this point.

The peak rectifier Gl 602 obtains from the 50 kHz section the reference voltage for the subsequent differential amplifier. The peak rectification has the advantage of excellent frequency response, but requires a low distortion supply voltage.

Before the 50 kHz voltage reaches Gl 602 it passes the dB/dBm divider. In voltage level setting (drawing of Rel. 607) the 50 kHz voltage is present directly at rectifier Gl 602, in power level position the 50 kHz voltage is stepped down.

On the first divider board 340 AB, also at the point of application of the peak rectifier Gl 601, is mounted the ohmic divider for output II. This output has a resistance of R_i= 75 Ohm and fixed division at $R_a = R_i$ of a = 10 dB.

The test plug St 603 is used for testing the module. Here the input signal can be observed at the point of application of rectifier Gl 601.

Any divisions in 10 dB steps between a = 0 dB and a = 70 dB can be adjusted with the divider transformers in the main signal path to output I. The cor-

responding switchover of the transformers is effected by relays which are controlled through the output level switch (22).

The inductances L 601 ... L 603 and L 608 are used to render line and leakage inductance between the output of the 30 dB divider board 340-AC 1 and the rectifier Gl 601 the same for all divider settings. This is necessary in order to make the reflection factor independent of the divider setting.

Board 610-D incorporates the 2 :1 transformer for R_i=0 and a correction element which compensates the leakage inductance and additional inductances and thus represents a frequency independent internal resistance of 75 Ohms. C 603 is used for frequency response correction, C 604 is used for adjustment of the reflection factor for the 75 Ohm position.

The adjustable load resistors after the tappings of the divider transformers are used to reduce the frequency response increasing at high frequencies as a result of resonance of the control inductance with the circuit capacitance.

The resistor R 604 alters the 50 Ohm internal resistance so that the resultant error is of the magnitude of the error at R_i= O (through coil resistors of the 2:1 transformer). By this means it is possible to ensure that the error when switching over from R_i= O to R_i= 75 Ohm becomes extremely small.

10.21. Output level switch (22)

The output level switch has 40 switch positions. It is thus possible to set an output level from O to -78 dB in stages of 2 dB each. This output level is valid with an instrument display of O dB. With the aid of the setting "Transmission level fine" (P 703) the transmission level can be reduced by a further 20 dB.

The divider errors of the output level switch are = 0.1 dB. The 2 dB stages are connected in a 50 kHz section, i.e. the reference voltage for the transmission level regulation is varied in 2 dB steps, thus the transmission level follows as well in 2 dB steps. After 4 stages on the output level switch a 10 dB coarse stage (transformer) is switched on in the output section and the 2 dB divider starts again at division O. The 10 dB coarse divisions in the output section cover the divisions from O to 60 dB by suitable series connection of divider transformers.

If the set is switched over to power level (dBm) an output level increased by 6 dB appears in the display window of the output level switch. The exact matching of the transmission level to the internal resistance (R_i= 75 Ohm) takes place in the 5o kHz branch and a transformer (Ü 608)which is located in the output section.

10.22. Carrier synchronous tuning 24 to 42.6 MHz (8)

In external control setting (S 801 position 1) the 24 to 42.6 MHz carrier signal coming from the receiver is passed through Bu 801 to the carrier external control. The signal voltage occurring at Bu 801 is 120 mV. From here the control signal is passed through transformer Ü 801 to the actual carrier external control. Transformer Ü 801 and insulated jack Bu 801 are intended to prevent any additional low resistance chassis connection occurring between transmitter and receiver through the external control cable. R 810 applies the lead to chassis potential. For improvement of the signal-to-noise ratio balancing for Ü 801 with C 810 and Ü 802 has been introduced (340-BC). In addition, for attenuation of interference by external high frequency fields, a further band pass filter (340-Y3) has been incorporated for the carrier frequency 24 to 42.6 MHz.

The external control input is designed for Z = 75 Ohm. R 801/82 Ohm/R 805/ 3.9 kOhm form the 75 Ohm terminating resistance. For suppression of 1 MHz interference a high-pass filter (∝/1) has been used, this being formed by L 805,C 806 and R_a = 300 Ohm (R 803/ R 802/Re_T).

Its cut-off frequency is approximately 15 MHz. The gain of stage T 802 is V = 15 dB. Through the collector stage T 801 the carrier signal is coupled out and again passed to a limiter and collector stage(Gl 1610, T 1607) located in the carrier oscillator. This stage receives its current supply at the same time as the signal.

So that in normal operation (without external control with external control cables plugged in no interference occurs as a result of cross-talk, Rel. 801 is switched off in this operating state. As this alone however, with a required cross talk attenuation of 80 dB, will not suffice, the power supply for the entire carrier external control is additionally interrupted.

10. DESCRIPTION OF FUNCTION

In addition in normal operation diode Gl 1611 in the carrier oscillator is blocked which guarantees additional cross talk attenuation.

10.23. 1 MHz remote control (19)

In external control position the 1 MHz signal coming from the receiver is passed through Bu 1901 to the 1 MHz external control.

The signal voltage occurring at Bu 1901 is 200 mV. The input jack Bu 1901 from the transmitter is also insulated. The reasons are the same as described in the carrier external control.

The external control input is designed for Z = 75 Ohm. At the output of T 1903 a low pass filter C 1909, L 1902 is used whose cut-off frequency is 1.2 MHz. The low-pass filter has the function of suppressing multiples of 1 MHz as well as the carrier frequency. Through the base stage T 1902 the 1 MHz control signal is now passed to the pulse shaper (11). The capacitor C 1910 at the collector of T 1902 belongs to the 1 MHz circuit Ü 1101 in the pulse shaper.

So that in normal operation, with external control leads plugged in, the cross talk attenuation is sufficiently high, ≙ 80 dB being required, the 1 MHz control output of the receiver is supplied DC currentwise from stage T 1901 in the transmitter. The feedback of the DC current takes place through the screening of the carrier external control cable and resistor R 810.

If therefore in normal operation the supply voltage of T 1901 is switched off, the power supply for the output stage in the receiver is interrupted at the same time. As this as well does not fulfil the required 80 dB attenuation, the complete 1 MHz external control is additionally isolated from the power supply.

10.24. Blanking circuit (24)

The blanking circuit is a control circuit for gradual blanking of the transmission level and for switching off the indicator.

It consists of a number of transistor switches and a Schmitt trigger.

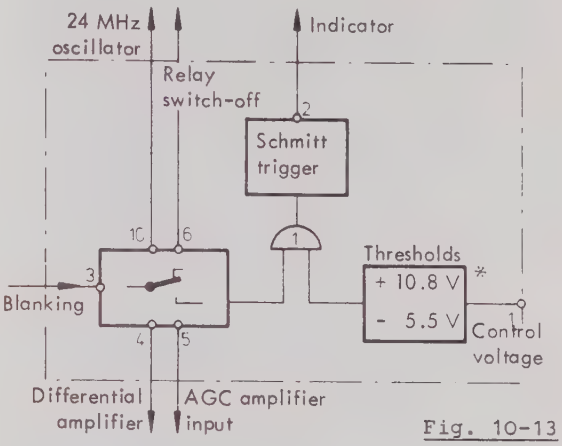


Fig. 10-13

*) The circuit emits a signal when the control voltage exceeds the stated limits.

In normal operation the following states prevail:
T 2401 is conductive whereby an emitter voltage of -5.2 V is obtained. T 2402 is blocked whereby -12V is obtained at the base of T 2403 - i.e. T 2403 is also blocked. Thus a voltage of 0 V results at the collector of T 2403. T 2404 is connected with the base through 270 kOhm to chassis and is conductive as Gl 2403 blocks. The basis therefore 2 thresholds (E_{BE} + E_S Gl 2404) more positive than the supply voltage (-12V). At the collector of T 2404 therefore -11.4 V results, whereby transistor T 405 becomes conductive through R 2428 and Gl 2414. As the Darlington stage T 2406 and T 2407 is blocked thereby, a voltage of +12V is obtained at TP 2401. This voltage is the supply voltage for the 24 MHz oscillator and the relays Rel. 601 - 606.

The Schmitt trigger (T 2408 and T 2409) switches off the indicator. It is activated by two points which are linked an OR-function, on the one hand by diode Gl 2405 with R 2415 as series resistor and in the second instance by emitter follower T 2411 with R 2416 as series resistor. Diode Gl 2412 with R 2425 ensures that for return to position of rest of the trigger after response the base of T 2409 has approximately the same R_i, the emitter follower is blocked in this operating mode. Activation of the trigger through T 2411 only takes place when the differential amplifier is overdriven positively or negatively. The switching thresholds at point 1 are +10.8 V and -5.5 V. The two capacitors C 2406 and C 2407 are intended to prevent interference peaks on the supply voltage causing the trigger to respond.

10. DESCRIPTION OF FUNCTION

During blanking the following takes place:
T 2401 blocks, T 2402 becomes conductive - an emitter voltage of - 5.6V results. R 2401 and C 2402 prevent uncontrolled blanking as a result of chatter of the blanking contact. Gl 2401 with C 2403 ensure high capacitance (Miller capacitor) at the base of T 2403. As a result the voltage at the collector of T 2403 moves in linear fashion to -11.6 V (Gl 2402 is blocked: it assumes the current during recharging of C 2403). The delay time of the collector voltages of T 2403 is approx. 4.6 ms. Whilst the collector potential drops, T 2405 is blocked and somewhat later T 2406/ T 2407 opens. The two Zener-diodes have the effect that T 2405 and T 2406/ T 2407 cannot conduct simultaneously. This would result in breakdown of the supply voltage as +12V and -12V would be momentarily short circuited through R 2413 (220 Ohm).

- 6V is now present at TP 2401, i.e. the relays in the output section drop out apart from Rel. 606.

The 24 MHz level induced by the negative voltage at point 4 now disappears completely as a result of switching off the 24 MHz oscillator through Gl 2413 and point 10.

The Schmitt trigger is switched by R 2415 and Gl 2405. As now T 2408 is conductive, current is removed from the indicator - it switches off.

If the Schmitt trigger is activated by the differential amplifier through point 1 (control circuit overdriven), two instances can be distinguished. If the voltage at point 1 is positive, T 2410 blocks as from +10.8 V and the base of T 2411 will be drawn to minus through R 2423 and Gl 2409.

T 2411 becomes conductive, the Schmitt trigger switches. If the voltage at point 1 becomes less than -5.5 V, the base of T 2411 is drawn to minus through Gl 2410 and R 2426 and the Schmitt trigger switches as above. Worthy of special mention is the circuit of T 2412.

The breakdown voltage of the base emitter diode is used as Zener-voltage. The advantage here lies in the fact that the stabilizing action is achieved at very low currents (50 - 100 µA).

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